5024 82065

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

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Date 12/6/02 Serial # 10/015,847 Priority Application Date 12/10/01

Your Name M. Lewis Examiner # _____

AU 2829 Phone 305-3743 Room _____

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

Th EIC s archer normally will contact you before beginning a prior art search. If you would like to sit with a s archer for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

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What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___ _____
Teaching Refs ___ _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-12

Problem: See Page 1 lines 10-21
" " 2 " 1-21

Solution See Page 3 " 1-24
" " 9 " 1-13

Staff Use Only

Searcher: Shackford
Searcher Phone: 308-0559
Searcher Location: STIC-EIC2800, CP4-9C18
Date Searcher Picked Up: 12/10/02
Date Completed: 12/10/02
Searcher Prep/Rev Time: 30
Online Time: 70

Type of Search

Structure (#)_____
Bibliographic ✓
Litigation_____
Fulltext_____
Patent Family_____
Other ✓

Vendors

STN ✓
Dialog ✓
Questel/Orbit_____
Lexis-Nexis_____
WWW/Internet ✓
Other _____

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 10dec02 13:56:49 User267149 Session D456.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Dec W2
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*File   2: Alert feature enhanced for multiple files, duplicates
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removal, customized scheduling. See HELP ALERT.
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removal, customized scheduling. See HELP ALERT.
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removal, customized scheduling. See HELP ALERT.
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  File  94:JICST-EPlus  1985-2002/Oct W1
         (c)2002 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Oct
         (c) 2002 The HW Wilson Co.
  File 144:Pascal  1973-2002/Dec W2
         (c) 2002 INIST/CNRS
  File 305:Analytical Abstracts  1980-2002/Nov W4
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Nov
         (c) 2002 DECHEMA
  File 350:Derwent WPIX  1963-2002/UD,UM &UP=200279
         (c) 2002  Thomson Derwent
*File 350: Alerts can now have images sent via all delivery methods.
See HELP ALERT and HELP PRINT for more info.
  File 347:JAPIO  Oct 1976-2002/Aug(Updated 021203)
         (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2002/Oct
         (c) 2002 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	2413719	SEMICONDUCT????????
S2	7344	CC=B2560 Semiconductor devices
S3	5227	MC=S01-G02B
S4	101968	IC=G01R-031
S5	2493290	S1:S4
S6	406029	MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N(-)MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR C(-)MOS? ? OR CMOS? ? OR NMOSFET? ? OR NMOS()FET? ?
S7	100903	DMOS()FET? ? OR DMOSFET? ? OR UMOS()FET? ? OR UMOSFET? ? OR MOS()FET? ? OR MOSFET? ?
S8	170226	(FIELD()EFFECT? ?(1W)TRANSIST???????) OR FET
S9	54686	CC=B2560R OR MC=S01-G02B OR IC=(G01R-031/26 OR G01R-031/27)
S10	606056	S6:S9
S11	331654	HIGH???()(VOLT? OR POWER?)
S12	99919	(DUAL OR TWO OR DOUBLE OR SECOND)(3N)(GATE? ? OR OPENING? -?)
S13	14111	OXIDE?(3N)(VOLT? OR POWER?)
S14	442868	S11:S13
S15	1937127	SUBSTRATE? ?
S16	235504	CC=(A6855 OR A8115 OR B0520 OR B2570) OR MC=(T03-A01B OR T-03-A01B1) OR IC=G11B-005/704
S17	2093055	S15:S16
S18	330947	OXIDE?(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S19	6787	BURIED(3N)OXIDE?
S20	334461	S18:S19
S21	72349	TOP(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S22	2857	TOP(3N)OXIDE?
S23	73631	S21:S22
S24	43435	GATE??(3N)OXIDE?
S25	362334	(SILICON OR SI)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S26	42935	SOI
S27	397316	S25:S26
S28	76011	SOURCE?(3N)(REGION??? OR AREA? ?)
S29	101841	BODY(3N)(REGION??? OR AREA? ?)
S30	5305	DRIFT(3N)(REGION??? OR AREA? ?)
S31	338492	S5 AND S10
S32	22516	S31 AND S14
S33	6716	S32 AND S17
S34	1968	S33 AND S20
S35	87	S34 AND S23
S36	35	S35 AND S24
S37	28	S36 AND S27
S38	17	S37 AND S28
S39	17	RD (unique items)
S40	2	S39 AND S29
S41	15	S39 NOT S40
S42	2	S41 AND S30
S43	13	S41 NOT S42
S44	11	S37 NOT S38
S45	11	S44 AND S10
S46	11	S45 AND S25
S47	11	RD (unique items)
S48	7	S36 NOT S37

S49 7 RD (unique items)

40/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013858503
WPI Acc No: 2001-342716/200136
Related WPI Acc No: 2000-349416
XRAM Acc No: C01-105967
XRPX Acc No: N01-248201
Semiconductor device in silicon **substrate** of first conductivity has trench, first and overlaying insulating **layers**, regions of **polysilicon** and second conductivity type, impurities region of first conductivity and conductive layer
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: LIZOTTE S C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6229194	B1	20010508	US 98114546	A	19980713	200136	B
			US 2000481045	A	20000111		

Priority Applications (No Type Date): US 98114546 A 19980713; US 2000481045 A 20000111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6229194	B1		17	H01L-029/00	Div ex application US 98114546 Div ex patent US 6054365

Abstract (Basic): US 6229194 B1
Abstract (Basic):
NOVELTY - A **semiconductor** device in silicon **substrate** of first conductivity type comprises trench separating and surrounding each cell in **substrate**; first insulating layer on lower portion of trench walls; regions of polysilicon and second conductivity type; impurities region of first conductivity type; overlaying insulation layer having openings; and conductive layer having interconnecting contacts.

DETAILED DESCRIPTION - A **semiconductor** device in silicon **substrate** of first conductivity type consists of trench, first insulating **layer** (50), region of **polysilicon**, region of second conductivity type, impurities region of first conductivity type, overlaying insulation layer (60), and conductive layer. The trench separates and surrounds each of at least two cells in the **substrate** and extends from the top to the bottom surface of the **substrate**. The first insulating layer is formed only on a lower portion of the trench walls and arranged so that an upper portion of the trench walls remains free. The region of polysilicon is formed in the trench and extends from top to bottom surface of the **substrate** between the insulating material layer. The region of second conductivity type is formed on the top surface of silicon **substrate**. The impurities region of first conductivity type is formed on top surface of the **substrate** and is spaced from and surrounds the region of second conductivity type. The overlaying insulation **layer** on **top** surface of the **substrate** has opening(s) to the region of first conductivity type in one of the cells and to the region of second conductivity type adjoining one of the cells. The conductive layer comprises interconnecting contact(s), which

connect the regions of first conductivity type of the respective cell and second conductivity type of the adjoining cell.

USE - Used as **semiconductor** device e.g. photovoltaic generator, **metal oxide semiconductor field effect transistors** or isolated gate bipolar transistors.

ADVANTAGE - The device is formed using simple and inexpensive starting wafer so reducing its cost. The more expensive processing steps, e.g. trench formation and trench filling with dielectric and polysilicon, can be formed towards the end of the process.

DESCRIPTION OF DRAWING(S) - The figures show the device.

First insulating layer (50)

Second insulating layer (51)

Overlaying insulation layer (60)

Passivation layer (80)

pp; 17 DwgNo 5, 6/11

gate, and a metal layer in contact with the top surface of the body. The gate is bordered by a **gate oxide layer** comprising a first portion adjacent the channel region and a thicker **second** portion overlying the **gate**.

DETAILED DESCRIPTION - A trench-gated power **MOSFET** comprises a **semiconductor** body having a trench, a gate disposed in the trench, and a metal layer (269) in contact with the top surface of the body. The trench wall intersects a major surface of the body at a trench corner. The **body** has a **source region** of a first conductivity type adjacent the trench and major surface of the **body**, a **body region** of a second conductivity type forming a junction with the **source region**, and a drain region of a first conductivity type forming junction of the **body region**. The **body region** has a channel region adjacent the trench wall. The gate is bordered by a **gate oxide layer** comprising a first portion adjacent the channel region and a thicker **second** portion overlying the **gate**. The contact between metal **layer** and **top** surface extend laterally to the trench corner.

An INDEPENDENT CLAIM is also included for a process of fabricating a trench **MOSFET** comprising: forming a first mask over a body surface of **semiconductor** material; etching the **semiconductor** material (267) through an opening of the mask to from a trench in the body; forming a first **oxide layer** in the trench; introducing **polysilicon layer** into the trench; oxidizing an exposed surface of the polysilicon to form second **oxide layer** at the **top** of the trench; removing the mask, and depositing a metal layer on a surface of the second **oxide layer** and the body.

USE - Used as a switch.

ADVANTAGE - The first portion of the **gate oxide layer** prevents shorting between the gate and source, thus allowing the contact between the metal layer and major surface to extend to the corner of the trench. The contact is self-aligned to the trench without the risk of a gate-source short and the design rules can be avoided and the width of the mesa between segments of the trench can be made smaller than was possible with conventional **MOSFET**'s. The cell density is increased and the figure of merit A/W is reduced.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional views of the invention.

Semiconductor material (267)
Metal layer (269)
Nitride layer (276)
Substrate (300)
pp; 105 DwgNo 24P/28

42/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014404049
WPI Acc No: 2002-224752/200228
XRAM Acc No: C02-068518
XRPX Acc No: N02-172211
High voltage semiconductor device e.g., complementary **metal oxide semiconductor** transistor, is formed by forming gate electrode in trenches at same height as top surfaces of **source** and drain **regions** of different doping densities
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: TUNG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6319776	B1	20011120	US 99310238	A	19990512	200228	B

Priority Applications (No Type Date): US 99310238 A 19990512
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6319776	B1		8	H01L-021/336	

Abstract (Basic): US 6319776 B1
Abstract (Basic):
NOVELTY - Doping regions (120, 121, 130, 131) with different doping densities are formed within **source** and drain **regions** (200, 210) of a **substrate** (100). Trenches (A, B) are formed inside the **substrate**, and a gate electrode (190) is buried within the trenches, such that the top surfaces of buried gate electrode and the **source** and drain **regions** are at same height.
USE - The method is used for manufacture of **high voltage** complementary **metal oxide semiconductor** (**CMOS**) transistor used in ultra high density integrated circuit.
ADVANTAGE - Since the channel and **drift regions** are placed vertically, chip area is reduced. Since the doping regions have different doping densities, device is capable of handling **high voltages**, and current capability is increased.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **semiconductor** device under fabricating process.
Substrate (100)
Doping regions (120, 121, 130, 131)
Gate electrode (190)
Source region (200)
Drain region (210)
pp; 8 DwgNo 2L/2

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014696500
WPI Acc No: 2002-517204/200255
XRAM Acc No: C02-146325
XRPX Acc No: N02-409172
Formation of self-aligned vertical double gas **metal oxide semiconductor field effect transistor** device involves growing **oxide layer** on surface of **silicon** -on-insulator **substrate** having **buried oxide** region
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CROWDER S; HARGROVE M J; KU S H; LOGAN L R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6372559	B1	20020416	US 2000709073	A	20001109	200255	B

Priority Applications (No Type Date): US 2000709073 A 20001109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6372559	B1		9	H01L-021/00	

Abstract (Basic): US 6372559 B1
Abstract (Basic):

NOVELTY - A self-aligned vertical double gas **metal oxide semiconductor field effect transistor** device is fabricated by growing an **oxide layer** on a surface of silicon-on-insulator **substrate** having **buried oxide** region between a **top silicon** -containing **layer** and bottom **silicon**-containing **layer** of the same conductivity type.

DETAILED DESCRIPTION - Formation of self-aligned vertical double gas **metal oxide semiconductor field effect transistor** (**MOSFET**) device comprises growing an **oxide layer** on a surface of silicon-on-insulator (**SOI**) **substrate** having **buried oxide** region (16) between a **top silicon**- (**Si**) containing **layer** and bottom **Si**-containing **layer** of the same conductivity type. The **gate** openings in the **oxide layer**, **top Si**-containing **layer** (14) and **buried oxide** region are patterned and etched until the bottom **Si**-containing **layer**. A gate dielectric (22) is formed on the exposed vertical sidewalls of the gate openings and the gate openings are filled with Si. An oxide is removed on horizontal surfaces, which interface with the **Si**-containing bottom **layer**. The **Si** interfaced to the gate dielectric is recrystallized and the gate openings are filled with epitaxial silicon. A mask is formed on the **oxide layer** so as to cover the silicon filled gate openings, while leaving an adjacent exposed silicon filled gate opening. Dopants of first conductivity-type is selectively implanted into the exposed silicon filled gate opening and then activated. The dopants are implanted at ion dosage of at least1x1015/cm2. The exposed **oxide layer** and underlying **top Si**-containing **layer** are selectively etched. The etching is stopped on the **buried oxide layer**. The mask is removed and a graded-channel

dopant profile is removed in the previously covered silicon filled **gate** opening. Any remaining **oxide layer** is etched and spacers (40) are formed about the silicon filled gate openings. Any exposed silicon surfaces are salicided.

USE - For forming a self-aligned vertical double gas **MOSFET** device.

ADVANTAGE - The inventive method is simple yet effective in fabricating **double-gate** devices, which is capable of forming self-aligned gates and well-controlled vertical asymmetrical channel-doping profile, while decoupling the gate contact implant/anneal from the processing steps used in forming the intrinsic device. All gate and drain anneals may be optimized for highest possible activation. The inventive method is complementary **metal oxide semiconductor** (**CMOS**)- compatible with p-**field effect transistor** (pFET) processing. It achieves smaller dimensions with better control.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the inventive **double gate MOSFET** device fabricated through the inventive method

Top Si-containing **layer** (14)
Buried oxide region (16)
Gate dielectric (22)
Spacers (40)
pp; 9 DwgNo 7/7

42/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012456969
WPI Acc No: 1999-263077/199922
XRAM Acc No: C99-077503
XRPX Acc No: N99-195911
Fabrication of complementary **metal oxide semiconductor** (**CMOS**) transistor
Patent Assignee: HONEYWELL INC (HONE)
Inventor: KUENG J S; ROISEN R L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5893729	A	19990413	US 95495141	A	19950628	199922 B
			US 96671100	A	19960628	

Priority Applications (No Type Date): US 95495141 A 19950628; US 96671100 A 19960628
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5893729	A		9	H01L-021/00	Cont of application US 95495141

Abstract (Basic): US 5893729 A
Abstract (Basic):
NOVELTY - Method for forming a complementary **metal oxide semiconductor** (**CMOS**) transistor in a **silicon layer** above an underlying **buried oxide layer** comprises:
(a) isolating first and second active areas in the **silicon layer**;
(b) forming n-well and p-well in the first and second active areas respectively, with first and **second gates** over them;
(c) forming lightly doped drain region in the **silicon layer** adjacent the **second gate** and extending through the thickness of the **silicon layer**; and
(d) forming **source** and drain **regions** in the p-well with the p-well spaced apart from a first edge of the **second gate** to provide an extended **drift region**.
USE - **CMOS** circuits for high temperature and **high power** applications.
ADVANTAGE - The use of variable width trench isolation eliminates the need for a conventional field oxide channel stop implant to prevent leakage between n-channel transistors. This allows a device which will function reliably at both at least 350 degreesC and with power supplies at least 14 V.
DESCRIPTION OF DRAWING(S) - The drawing shows the **MOS** device.

p-substrate (40)
buried oxide layer (42)
source (16)
drain (18)
top silicon layer (44)
channel region (46)
gate oxide (50)
spacers (52, 54)

40/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013531670
WPI Acc No: 2001-015876/200102
XRAM Acc No: C01-004307
XRPX Acc No: N01-012016
Trench-**gated** power **metal oxide semiconductor field-effect transistor** used as a switch has **semiconductor** body with trench, **gate** bordered by **gate oxide layer**, and metal **layer** in contact with major surface of the body
Patent Assignee: GRABOWSKI W (GRAB-I); WILLIAMS R K (WILL-I); ADVANCED ANALOGIC TECHNOLOGIES INC (ADAN-N)
Inventor: GRABOWSKI W; WILLIAMS R K
Number of Countries: 091 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200065646	A1	20001102	WO 2000US10770	A	20000421	200102	B
AU 200048001	A	20001110	AU 200048001	A	20000421	200109	
US 20020019099	A1	20020214	US 99296959	A	19990422	200214	
EP 1186023	A1	20020313	EP 2000930123	A	20000421	200225	
			WO 2000US10770	A	20000421		
KR 2001112439	A	20011220	KR 2001713334	A	20011019	200239	
US 6413822	B2	20020702	US 99296959	A	19990422	200248	
CN 1353863	A	20020612	CN 2000808393	A	20000421	200262	
US 20020168821	A1	20021114	US 99296959	A	19990422	200277	
			US 2002146568	A	20020514		

Priority Applications (No Type Date): US 99296959 A 19990422; US 2002146568 A 20020514
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200065646	A1	E	105	H01L-021/76	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 200048001	A		H01L-021/76	Based on patent WO 200065646
US 20020019099	A1		H01L-021/336	
EP 1186023	A1	E	H01L-021/76	Based on patent WO 200065646

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

KR 2001112439	A		H01L-029/76	
US 6413822	B2		H01L-021/336	
CN 1353863	A		H01L-021/76	
US 20020168821	A1		H01L-021/336	Cont of application US 99296959
				Cont of patent US 6413822

Abstract (Basic): WO 200065646 A1
Abstract (Basic):
NOVELTY - A trench-**gated power metal oxide semiconductor field effect-transistor** (**MOSFET**) comprises a **semiconductor** body having a trench, a

43/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014860429
WPI Acc No: 2002-681135/200273
XRAM Acc No: C02-192145
XRPX Acc No: N02-537615
Memory array and support transistor formation on **semiconductor substrate** comprises forming silicide layers on **source**/drain **regions** and on **polysilicon layer** overlying bitline diffusion regions and defining landing pad
Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (INFN); INT BUSINESS MACHINES CORP (IBMC)
Inventor: DIVAKARUNI R; GRUENING U; MANDELMAN J A; NESBIT L; RADENS C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6429068	B1	20020806	US 2001897868	A	20010702	200273	B

Priority Applications (No Type Date): US 2001897868 A 20010702
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6429068	B1		18	H01L-021/8242	

Abstract (Basic): US 6429068 B1
Abstract (Basic):
NOVELTY - Forming a memory array and support transistors on a **semiconductor substrate** comprises simultaneously forming silicide layers on an exposed portion of **source** and drain **regions** in the support region, on the second **polysilicon layer** overlying bitline diffusion regions in the array region, and on the second **polysilicon layer** defining a landing pad.

DETAILED DESCRIPTION - Forming a memory array and support transistors on a **semiconductor substrate** (202) comprises providing a memory structure having an array region and a support region separated by an isolation region (208). The array region includes dynamic random access memory cells embedded in the **substrate**. Adjacent random access memory cells are connected to each other through bitline diffusion regions (214). The memory structure is capped with a **top oxide layer** (210). A block mask is applied to protect the array region while stripping the **top oxide layer** from the support region. Support implants and a support **gate oxide layer** are formed. A first **polysilicon layer** (302) is patterned onto the support **gate oxide layer**. A conductive nitride barrier layer (250), a metal layer (252) and a dielectric capping layer (254) are formed on all exposed surfaces of the **substrate**. Portions of the nitride barrier layer, metal layer and dielectric capping layer are removed from the support region to form a support gate structure. The nitride barrier layer, metal layer and dielectric capping layer are removed from the isolation region. The support gate structure comprises the **gate oxide layer**, first **polysilicon layer**, nitride barrier **layer**, metal layer, and dielectric capping layer. An insulated spacer is formed on sidewalls of the gate structure. A protective layer is formed on all exposed surfaces of the **substrate**. An array gate structure is formed in contact with the memory cell. A portion of the bitline diffusion region is exposed by

removing portions of the protective layer, the nitride barrier layer, the metal layer and the dielectric capping layer from the array region. The array **gate** structure comprises the **oxide layer**, the nitride barrier layer, the metal layer and the dielectric capping layer. The protective layer is simultaneously removed from the isolation region. A spacer layer is formed on sidewalls of the array **gate** structure. A **second polysilicon layer** is deposited onto the **substrate**. It is selectively patterned and etched in the isolation region to form a landing pad while the **polysilicon layer** is removed from the support regions. Silicide layers are simultaneously formed on an exposed portion of the **source** and drain **regions** in the support region, on the second **polysilicon layer** overlying the bitline diffusion regions in the array region, and on the second **polysilicon layer** defining the landing pad.

USE - For the production of embedded vertical **MOSFET** dynamic random access memory (DRAM) cells.

ADVANTAGE - The process eliminates the need for a metallization layer which is the most difficult layer to photolithographically pattern. Reliance on complicated optical proximity correction schemes and alternating phase shift masking techniques is reduced.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view illustrating the production of a DRAM array and supports.

Substrate (202)
Isolation region (208)
Top oxide layer (210)
Bitline diffusion regions (214)
Nitride barrier layer (250)
Metal layer (252)
Dielectric capping layer (254)
Polysilicon layer (302)
pp; 18 DwgNo 10/10

43/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014686714
WPI Acc No: 2002-507418/200254
Related WPI Acc No: 2002-214352
XRAM Acc No: C02-144235
XRPX Acc No: N02-401538
Formation of dual work function **metal oxide semiconductor field effect transistor**/embedded dynamic random access memory array by removing exposed second **polysilicon layer** while removing exposed portions of first **polysilicon layer**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DIVAKARUNI R; MANDELMAN J A; RADENS C·J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020055224	A1	20020509	US 2000706492	A	20001103	200254 B
			US 2001862827	A	20010522	

Priority Applications (No Type Date): US 2000706492 A 20001103; US 2001862827 A 20010522
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020055224	A1		24	H01L-021/8242	Div ex application US 2000706492

Abstract (Basic): US 20020055224 A1
Abstract (Basic):

NOVELTY - A dual workfunction high performance **metal oxide semiconductor field effect transistor**/embedded dynamic random access memory array is formed by removing an exposed second **polysilicon layer** from an isolation region, while simultaneously removing exposed portions of a first **polysilicon layer** in a support region(s) in which a gate conductor guard ring is formed on the isolation region.

DETAILED DESCRIPTION - Formation of a dual workfunction high performance **metal oxide semiconductor field effect transistor**/embedded dynamic random access memory (**MOSFET**/EDRAM) array having a gate conductor (30) guard ring formed around the array region, comprises providing a memory structure having an array region(s) and a support region(s) which are separated by an isolation region (16). The array region(s) includes DRAM cells embedded in a **substrate** (18). Adjacent DRAM cells are connected to each other through bitline diffusion regions (22) which are capped with an **oxide** capping **layer** (44). A patterned nitride layer is formed on all exposed surfaces in the array region(s) and on a portion of the isolation region. A **gate oxide** is formed on the **substrate** in the support region(s). A stack comprising a first **polysilicon layer** (42) and a dielectric capping layer (56) is formed on all exposed surfaces of the memory structure. The dielectric capping **layer**, the first **polysilicon layer** , and the nitride layer are removed from the array region(s). Wordlines (52) are formed on the DRAM cells in the array region(s). Spacers (58) are formed on exposed sidewalls of the wordlines, and on exposed sidewalls of the stack remaining in the structure. A block mask is

formed on a support region(s) and a portion of the DRAM cells that is adjacent to the isolation region. It does not cover the **oxide** capping **layer**. The **oxide** capping **layer** on the bitline diffusion regions is removed, and the block mask is stripped. A patterned second **polysilicon layer** is formed on the array region and the stack which is present on the isolation region. The dielectric capping layer is removed in the support region(s). A doped glass material layer is formed on all surfaces in the array region(s) and the support region(s). The doped glass material layer is patterned to form hard masks in the array region(s) and the support region(s). The hard mask in the array region(s) defines a bitline of the memory structure, and the hard mask in the support region(s) defines a support **gate** region. The exposed **second polysilicon layer** is removed from the array region(s) and the isolation region, while simultaneously removing exposed portions of the first **polysilicon layer** in the support region(s) in which a gate conductor guard ring is formed on the isolation region, and the support gate region is formed in the support region(s). The hard masks are removed from an array region(s) and the support region(s), and a screen **oxide layer** (66) is formed on any exposed silicon surfaces. **Source** and drain **regions** (74) are formed on the support **gate** region(s). An **oxide** overlying the bitline, support gate **region**, and **source** and drain **regions**, is removed to expose silicon surfaces. The exposed silicon surfaces are salicided to provide salicide regions (76) on the bitline, the gate **region** and the **source** and drain **regions**.

USE - For the formation of dual workfunction high performance **MOSFET**/EDRAM.

ADVANTAGE - The method eliminates additional masking steps to form high performance complementary **metal oxide semiconductor** logic devices and borderless contacts. It does not share support gate conductor lithography with wordline lithography. It shares the gate conductor lithography with the array bitline lithography step. The presence of the guard ring provides an internal protection scheme, which prevents the designer from placing gate conductor across the isolation region.

DESCRIPTION OF DRAWING(S) - The figure shows a pictorial view of the processing step of the inventive method.

Isolation region (16)
Substrate (18)
Bitline diffusion regions (22)
Gate conductor (30)
Oxide capping **layer** (44)
First **polysilicon layer** (42)
Wordlines (52)
Conductive metal (54)
Dielectric capping layer (56)
Spacers (58)
Screen **oxide layer** (66)
Source and drain **regions** (74)
Salicide regions (76)
pp; 24 DwgNo 12/27

43/3,AB/3 (Item 3 from file: 350)

014253571
WPI Acc No: 2002-074271/200210
XRAM Acc No: C02-021971
XRPX Acc No: N02-054761
Manufacture of bipolar-complementary **metal oxide semiconductor** device by forming N well region for P channel devices, forming P well region for N channel devices and using N type epitaxial **silicon layer** for NPN bipolar device
Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)
Inventor: CHANG K; TSUI B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6303419	B1	20011016	US 2000534165	A	20000324	200210	B

Priority Applications (No Type Date): US 2000534165 A 20000324
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6303419	B1		19	H01L-021/8238	

Abstract (Basic): US 6303419 B1
Abstract (Basic):

NOVELTY - A bipolar-complementary **metal oxide semiconductor** device is made by forming an N well region for P channel devices; forming a P well region for N channel devices; and using an N type epitaxial **silicon layer** for the NPN bipolar device. The N type epitaxial layer, in terms of dopant concentration, is specifically designed for the NPN bipolar devices.

DETAILED DESCRIPTION - Fabrication of a bipolar-complementary **metal oxide semiconductor** (BiCMOS) device on a **semiconductor substrate**, comprising N type **field effect transistor** (NFET) and P type **field effect transistor** (PFET) complementary oxide **semiconductor** (**CMOS**) devices; and an NPN bipolar junction transistor, all formed in, and on an N type, epitaxial **silicon layer**, comprises

(a) forming a buried N type layer, in a region of the **semiconductor substrate** to be used as a PFET **CMOS** region;

(b) forming an N type sub-collector region, in a region of the **semiconductor substrate**, to be used as a bipolar device region (62);

(c) forming a buried P type region, in a region of the **semiconductor substrate** to be used as an NFET **CMOS** region;

(d) growing the N type epitaxial **silicon layer**, on the **top** surface of the **semiconductor substrate**;

(e) forming an N well region, in a first area of the N type epitaxial **silicon layer**, with the N well region overlying, and contacting, the N type buried layer;

(f) forming an N type reach through region, in a second area of the N type epitaxial **silicon layer**, with the N type reach

through region, overlying and contacting a first portion of the N type sub-collector region;

(g) forming a P well region, in a third area of the N type epitaxial **silicon layer**, with the P well region overlying, and contacting, the buried P type layer;

(h) forming a first silicon dioxide isolation region, in a region of the **semiconductor substrate** located between the PFET **CMOS** region, and NFET **CMOS** region, and forming a second silicon dioxide isolation region, in a region of the **semiconductor substrate** located between the NFET **CMOS** region and the bipolar device region;

(i) growing a **silicon dioxide gate** insulator **layer** on regions of the **semiconductor substrate**, exposed between silicon dioxide isolation regions;

(j) depositing a thin **polysilicon layer** (19);

(k) forming a P type base region, in a top portion of the N type epitaxial **silicon layer**, in a region in which the N type epitaxial **silicon layer**, overlays a second portion of the N type sub-collector regionl) forming an emitter opening in the thin **polysilicon layer**, exposing a portion of the **silicon dioxide gate** insulator **layer**, residing on underlying P type base region;

(m) forming an N type self-aligned collector, (SIC), region, in a bottom portion of the N type epitaxial **silicon layer** (6), located underlying the P type base region, and overlying a portion of the N type sub-collector region, and with the N type SIC region, self aligned to overlying, the emitter opening;

(n) removing the portion of the **silicon dioxide gate** insulator **layer**, exposed in the emitter opening;

(o) depositing a thick **polysilicon layer**;

(p) doping of the thick **polysilicon layer**;

(q) patterning of the thick **polysilicon layer**, and of the thin **polysilicon layer** to form a first polysilicon gate structure, on the **silicon dioxide gate** insulator **layer**, in the PFET **CMOS** region; to form a **second** polysilicon **gate** structure, on the **silicon dioxide gate** insulator **layer**, in the NFET **CMOS** region; and to form a polysilicon emitter structure (28b), overlying and contacting a portion of the P type base region (21), exposed in the emitter opening;

(r) growing a **silicon oxide layer** on the exposed surfaces of the first polysilicon gate structure (26b); of the **second** polysilicon **gate** structure; and of the polysilicon emitter structure;

(s) forming a lightly doped, P type **source**/drain **region**, in an area of the PFET **CMOS** region, not covered by the first polysilicon gate structure;

(t) forming a lightly doped, N type **source**/drain **region** (30), in an area of the NFET **CMOS** region, not covered by the **second** polysilicon **gate** structure;

(u) forming insulator spacers on the sides of the first polysilicon gate structure; the sides of the **second** polysilicon **gate** structure; and on the sides of the polysilicon emitter structure;

(v) forming a heavily doped, P type **source**/drain **region** (36), in an area of the PFET **CMOS** region (60), not covered by the first polysilicon gate structure, or by the insulator spacers;

(w) forming a heavily doped, N type **source**/drain **region** (35), in an area of the NFET **CMOS** region, not covered by the

second polysilicon **gate** structure, or by the insulator spacers; and

(x) performing an emitter anneal cycle, creating an emitter region (34) top portion of the P type base region, exposed in emitter opening (23), resulting in a P type base width, located between overlying, the emitter region, and underlying, the N type SIC region (24).

USE - For isolating a BiCMOS device.

ADVANTAGE - The inventive method produces a BiCMOS structure that employs separate masks for the P well, as well as for the N well **CMOS** regions, while choosing the ideal N type epitaxial **silicon layer** for the NPN bipolar devices. It integrates (a) the fabrication of twin wells, a P well for the N type **CMOs** devices, and an N well for the P type **CMOS** devices, into the BiCMOS fabrication process; and (b) an N type, epitaxial layer, into the BiCMOS fabrication sequence, to be used as the collector region of the bipolar device.

DESCRIPTION OF DRAWING(S) - The figure shows the heavily doped, N type **source** drain **region** in NFET **CMOS** region and P type heavily doped **source**/drain **region** in PFET **CMOS** region.

N type epitaxial **silicon layer** (6)
Thin **polysilicon layer** (19)
P type base region (21)
Emitter opening (23)
N type SIC region (24)
Polysilicon gate structure (26b)
Polysilicon emitter structure (28b)
N type **source**/drain **region** (30)
Emitter region (34)
N type **source**/drain **region** (35P type **source**/drain **region** (36)
PFET **CMOS** region (60)
Bipolar device region (62)
pp; 19 DwgNo 16/16

43/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796518
WPI Acc No: 2001-280729/200129
Related WPI Acc No: 2000-686022
XRAM Acc No: C01-085170
XRPX Acc No: N01-200128
Manufacture of integrated circuit device i.e., complementary **metal oxide semiconductor** device, comprises etching gate material using pattern defined by hard mask formed from exposed patterning layer on gate material
Patent Assignee: INTEL CORP (ITLC)
Inventor: DAS S; LIANG C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6207541	B1	20010327	US 97862	A	19971230	200129	B
			US 99465549	A	19991216		

Priority Applications (No Type Date): US 97862 A 19971230; US 99465549 A 19991216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6207541	B1		8	H01L-021/3205	Div ex application US 97862 Div ex patent US 6133128

Abstract (Basic): US 6207541 B1
Abstract (Basic):
NOVELTY - Making an integrated circuit device comprises exposing a patterning layer formed on a surface of a gate material to form an **oxide layer**; developing the **oxide layer** to remove portion external to the pattern to expose a dielectric **layer top** surface; forming a hard mask having sidewalls from the **oxide layer**; etching the **gate** material according to the pattern defined by the hard mask.
DETAILED DESCRIPTION - Making an integrated circuit device comprises etching trenches in a surface of a **substrate** (102); growing a dielectric layer (104) on a surface of the **substrate**; depositing a gate material layer on a surface of the dielectric layer; forming a patterning layer on a surface of the gate material; exposing the patterning **layer** to form an **oxide layer**; developing the **oxide layer** to remove that portion external to the pattern of the patterning layer to expose a dielectric **layer top** surface; forming from the **oxide layer** a hard mask having sidewalls; etching the gate material layer according to the pattern defined by the hard mask to form a conducting gate (107) having sidewalls that are complementary to the hard mask side walls; forming **silicon** nitride **spacers** (116) along the dielectric **layer top** surface and the sidewalls of the conducting gate; removing the hard mask; forming active regions (103) at each trench by removing material from the gate material layer that is external to each dielectric **layer top** surface and external to the area underneath each gate; and forming **source regions**(s) (118) and drain regions(s) (119) in the **substrate** between a **gate** and **two** active regions.

USE - For making an integrated circuit device i.e., complementary **metal-oxide semiconductor** device (**CMOS**).

ADVANTAGE - The invention provides a process for patterning a gate of a transistor to obtain high image resolution while providing good photoresistance to etching. The process can be easily integrated into a standard **CMOS** fabrication process.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of an integrated circuit structure of the invention.

Substrate (102)
Active regions (103)
Dielectric layer (104)
Gate (107)
Spacers (116)
Source regions (118)
Drain regions (119)
Silicide (120)
pp; 8 DwgNo 10/11

43/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013492220
WPI Acc No: 2000-664163/200064
XRAM Acc No: C00-201172
XRPX Acc No: N00-492134
Metal oxide semiconductor field-effect transistor for microelectronic technology includes buried contacts on **substrate**, an **oxide layer** on the first buried contact, and extended **source**/drain **regions**
Patent Assignee: TEXAS INSTR ACER INC (TEXI)
Inventor: WU S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6127712	A	20001003	US 9883610	A	19980522	200064	B
			US 99346041	A	19990706		

Priority Applications (No Type Date): US 99346041 A 19990706; US 9883610 A 19980522
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6127712	A		10	H01L-029/76	CIP of application US 9883610

Abstract (Basic): US 6127712 A
Abstract (Basic):
NOVELTY - A **metal oxide semiconductor field -effect transistor** (**MOSFET**) includes two buried contacts on a silicon **substrate** adjacent the sides of a **gate** dielectric **layer**; an **oxide layer** on the first contact; and extended **source**/drain **regions**. The poly **gate** and **second** buried contact form air gaps on **two** unoccupied **gate** dielectric layers.
DETAILED DESCRIPTION - A **MOSFET** with buried contacts and air-gap gate structure comprises a silicon **substrate** (102) with trench isolation regions (104) to define an active region; a poly gate (180a) formed of a **polysilicon layer** (180) in a mid portion of a gate dielectric layer so that there are **two** unoccupied **gate** dielectric layer at the sides of **polysilicon layer**; two buried contacts (140a-b) on the **substrate** adjacent on sides of the **gate** dielectric **layer**; an **oxide layer** (230) on **top** of the first buried contact, the poly **gate** and the **second** buried contact forming air gaps (235a-b) on the unoccupied gate dielectric layers (170a-b); two **source**/drain **regions** (240a-b) in the active region underneath the two buried contacts; and two extended **source**/drain **regions** (250a-b) being extended from the **source**/drain **regions** to **regions** underneath the unoccupied gate dielectric layers.
USE - The **MOSFET** is used for microelectronic technology.
ADVANTAGE - The ultra-short channel **MOSFET** is achieved in clarity defined by gate hollow. The device speed is improved due to reduced parasitic resistance by the extended source/drain junction and the parasitic gate fringe capacitor and the capacitance between

source/drain and gate is lowered by the air-gaps gate structure. The size of the transistor is reduced due to forming buried contacts on both the **source**/drain and STI **region**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **MOSFET** structure.

Silicon **substrate** (102)
Trench isolation regions (104)
Buried contacts (140a-b)
Gate dielectric layers (170a-b)
Polysilicon layer (180)
Poly gate (180a)
Oxide layer (230)
Air gaps (235a-b)
Source/drain **regions** (240a-b)
Extended **source**/drain **regions** (250a-b)
pp; 10 DwgNo 14/14

43/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013214899
WPI Acc No: 2000-386773/200033
Related WPI Acc No: 2000-023675
XRAM Acc No: C00-117217
XRPX Acc No: N00-289567
Lateral radio frequency **metal oxide semiconductor** device manufacture, comprises forming epi **silicon** layer, field **oxide layer, polysilicon gate, gate** channels, drain and **source regions** and connecting with outside circuitry
Patent Assignee: XEMOD INC (XEMO-N)
Inventor: D'ANNA P E
Number of Countries: 022 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6063678	A	20000516	US 9872393	A	19980504	200033	B
			US 99293431	A	19990416		
			US 99366612	A	19990731		
WO 200109938	A1	20010208	WO 99US20671	A	19990910	200110	

Priority Applications (No Type Date): US 99366612 A 19990731; US 9872393 A 19980504; US 99293431 A 19990416
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6063678	A		18	H01L-021/336	CIP of application US 9872393
					CIP of application US 99293431
WO 200109938	A1	E		H01L-021/336	

Designated States (National): CN FI JP KR SE
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Abstract (Basic): US 6063678 A
Abstract (Basic):
NOVELTY - Lateral radio frequency **metal oxide semiconductor** device is formed by growing an epi **silicon layer** over a **substrate** and a field **oxide layer** over the epi **layer**; and forming a **polysilicon** gate, gate channels, and **source** and drain **regions**. A silicided layer is formed on the polysilicon gate. Metal contacts connect the channels and the **source** and drain **regions** with an outside circuitry.
USE - For fabricating lateral radio frequency **metal oxide semiconductor** (RF **MOS**) device (10).
ADVANTAGE - Minimizes the electrical shorts between the polysilicon gate and the **source** and/or drain **areas**, and maximizes fabrication yield of lateral RF **MOS** devices per silicon wafer.
DESCRIPTION OF DRAWING(S) - The figure is a side view of a lateral RF **MOS** device having a non-diffusion connection between each **source region** and the **substrate**.
RF **MOS** device (10)
Substrate (12)
Epi layer (20)
Drain region (24)

43/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009445000
WPI Acc No: 1993-138519/199317
XRAM Acc No: C95-027219
XRPX Acc No: N95-048656
CMOS semiconductor devices mfg. methods - where N- and P-channel MISFETs are provided on a common **substrate**
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)
Inventor: INOKAWA H; KOBAYASHI T; MIYAKE M; MORIMOTO T; OKAZAKI Y
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 5075117	A	19930326	JP 91265298	A	19910917	199317	B
US 5382532	A	19950117	US 92946080	A	19920916	199509	
US 5585659	A	19961217	US 92946080	A	19920916	199705	
			US 94320690	A	19941011		

Priority Applications (No Type Date): JP 91265298 A 19910917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 5075117	A		25	H01L-029/784	
US 5382532	A	E	36	H01L-021/265	
US 5585659	A		37	H01L-029/76	Div ex application US 92946080 Div ex patent US 5382532

Abstract (Basic): US 5382532 A
Method of fabricating N-channel and P-channel MISFET's on a common **semiconductor substrate** comprising: (a) forming a first **gate oxide** on the **semiconductor substrate** for the N-channel MISFET; (b) depositing a **polysilicon film** doped with an N-type impurity for a first gate electrode of the N-channel MISFET over the entire surface of the **substrate**; (c) etching the **polysilicon film** deposited on the P-channel MISFET region (d) forming a **second gate oxide** of the P-channel and oxidising the surface of the **polysilicon film** remaining on the N-channel region after removal of the first **gate oxide**; (e) depositing a **polysilicon film** doped with a p-type impurity for a gate electrode of the P-channel MISFET over the entire surface; (f) eliminating at least a portion of the p-type **polysilicon film** deposited on a previously deposited n-type **polysilicon film** for the gate electrode of the N-channel MISFET except for a region around the terminus; and (g) forming a gate electrode pattern by simultaneously removing portions of the N-type and P-type **polysilicon films** using a resist mask to form the gate electrodes of the N and P channel MISFETs.
USE - Method for fabricating field-effect **semiconductor** devices having both N- and P-type MISFETs on a common **substrate**, e.g. a complementary-type-field effect **semiconductor** device.
ADVANTAGE - The off-characteristic, the short channel effect and the controllability of threshold voltage are progressed by providing both N and P channel MISFETs on a common **substrate**, and more specifically providing both **gates** with **dual** N+/P+ polysilicon **gate** structure, so that both N- and P-channel transistors are formed as surface channel type ones.

Dwg.1/68

Abstract (Equivalent): US 5585659 A

A complementary metal-insulator-**semiconductor** device comprising: a first transistor region having a first conductivity type and formed in a surface of a **semiconductor substrate**; a second transistor region having a second conductivity type which is opposite the first conductivity type, the second transistor region formed in the surface of the **semiconductor substrate** and isolated from the first transistor region; a first **field effect transistor** including: a) a first **gate oxide film** formed on the first transistor **region**; b) a **source region** and a drain region which are formed in the first transistor region; and c) a first gate **polysilicon film** having a **top** surface, the first gate **polysilicon film** being formed on the first **gate oxide film** and doped with an impurity having a conductivity type which is opposite the first conductivity type; a second **field effect transistor** including: a) a **second gate oxide film** formed on the second transistor **region**; b) a **source region** and a drain region which are formed in the second transistor region; and c) a **second gate polysilicon film** having a **top** surface, the **second gate polysilicon film** being formed on the **second gate oxide film** and doped with an impurity having a conductivity type which is opposite the second conductivity type; and an **oxide film** formed by an oxidation process, the **oxide film** is located between the first and **second gate polysilicon films** and has a **top** surface; and a silicide film or a refractory metal film being provided on and directly contacting a portion of the top surface of the first and **second gate polysilicon films** not covered by the **oxide film**, and being provided simultaneously on an exposed portion the **top** surface of the **oxide film**.

Dwg.1/68

43/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009273832
WPI Acc No: 1992-401243/199249
XRPX Acc No: N92-305980
MOS transistor with extended channel width - has parallel **oxide** protrusions beneath **gate** electrode in channel width direction
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: HWANG C; RHO B; HWANG C K; RHO B H
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2256315	A	19921202	GB 9118511	A	19910829	199249	B
DE 4127795	A	19921203	DE 4127795	A	19910822	199250	
JP 4368180	A	19921221	JP 91235678	A	19910823	199305	
IT 1250089	B	19950330	IT 91RM646	A	19910829	199537	

Priority Applications (No Type Date): KR 919066 A 19910531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2256315	A		33	H01L-029/784	
DE 4127795	A		13	H01L-029/784	
JP 4368180	A			H01L-029/784	
IT 1250089	B			G11C-000/00	

Abstract (Basic): GB 2256315 A

The **semiconductor** transistor comprises a **semiconductor substrate** of a first-conductive type, with **source** and drain **regions**, and an **oxide** insulating **layer**, formed on the **top** surface of the **substrate** having openings arranged in parallel in the direction of the channel width. A **semiconductor** layer fills the openings and has a thickness greater than that of the insulating layer. A conductive layer extends over the channel. Diffusion regions are formed in the **semiconductor** layer apart from underneath the conductive layer.

Pref. the **semiconductor layer** is a **silicon** epitaxial **layer**. Pref. the transistor further comprises **second openings** contacting metal electrodes over selected portion of the diffusion regions.

ADVANTAGE - Increased effective channel width, without increasing device area occupied on **substrate**. Improved current drive capability, controlled by oxide opening sidewall slope.

on
Dwg.2/9

43/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008946596
WPI Acc No: 1992-073865/199210
Related WPI Acc No: 1992-073882
XRAM Acc No: C92-033843
XRPX Acc No: N92-055561
Method for mfg. **double-gated MOS** transistor - with enhanced drive current and punch-through voltage resistance and reduced short-channel degradation and noise
Patent Assignee: SHARP KK (SHAF)
Inventor: ADAN A O; HORITA M; ADAN A O; ADAN A
Number of Countries: 008 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 473397	A	19920304	EP 91307833	A	19910827	199210	B
JP 4107832	A	19920409	JP 90227068	A	19900827	199221	
US 5145796	A	19920908	US 91749558	A	19910826	199239	
KR 9504842	B1	19950513	KR 9114768	A	19910826	199703	
EP 473397	B1	19980401	EP 91307833	A	19910827	199817	
DE 69129174	E	19980507	DE 629174	A	19910827	199824	
			EP 91307833	A	19910827		

Priority Applications (No Type Date): JP 90227068 A 19900827
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 473397	A		8		
Designated States (Regional): DE FR GB IT NL					
JP 4107832	A		4		
US 5145796	A		6	H01L-021/265	
EP 473397	B1	E	8	H01L-021/336	
Designated States (Regional): DE FR GB IT NL					
DE 69129174	E			H01L-021/336	Based on patent EP 473397
KR 9504842	B1			H01L-021/336	

Abstract (Basic): EP 473397 A

A method of mfg. **semiconductor** appts. comprising: (i) laminating first **polysilicon layer** on surface of **substrate** through first **oxide layer**; (ii) removing both layers in element sepn. region forming a trench, then retreat residual layers as a bottom gate electrode and insulating film respectively; (iii) forming monocrystalline **Si layer** by epitaxial growth on **substrate** and trenches; (iv) removing **Si layer** in element sepn. region, laminating second **oxide layer** on **substrate** making **oxide layer** remain as element sepn. film in only this region; and (v) forming **gate oxide film** and **top gate** electrode on bottom gate electrode through residual **silicon film** and forming source/drain on this film.

USE/ADVANTAGE - Method for mfg. **semiconductor** appts., partic. **Double-Gated MOS** Transistor. In a **Double-Gated CMOS** device drive current can be enhanced, higher punch-through voltage resistance is obtd. and short-channel degradation effects are reduced. Structure is resistant to **substrate** noise.

Dwg.1/2

Abstract (Equivalent): EP 473397 B

A method of mfg. **semiconductor** appts. comprising: (i) laminating first **polysilicon layer** on surface of **substrate** through first **oxide layer**; (ii) removing both layers in element sepn. region forming a trench, then retreat residual layers as a bottom gate electrode and insulating film respectively; (iii) forming monocrystalline **Si layer** by epitaxial growth on **substrate** and trenches; (iv) removing **Si layer** in element sepn. region, laminating second **oxide layer** on **substrate** making **oxide layer** remain as element sepn. film in only this region; and (v) forming **gate oxide film** and **top gate** electrode on bottom gate electrode through residual **silicon film** and forming source/drain on this film.

USE/ADVANTAGE - Method for mfg. **semiconductor** appts., partic. **Double-Gated MOS** Transistor. In a **Double-Gated CMOS** device drive current can be enhanced, higher punch-through voltage resistance is obtd. and short-channel degradation effects are reduced. Structure is resistant to **substrate** noise.

Dwg.0/2

Abstract (Equivalent): US 5145796 A

Method comprises (a) laminating a 1st **polysilicon layer** on the whole surface of a **semiconductor** through a 1st **oxide layer**; (b) removing the 1st **polysilicon** and 1st **oxide layers** in element sepn. regions to form trenches, and treating the residual layers as a bottom gate electrode and insulating film respectively; (c) forming a monocrystalline **Si layer** by epitaxial growth on the whole of the **substrate** including the trenches; (d) removing the mono-Si in the element sepn. regions to form openings, laminating a 2nd **oxide layer** on the whole **substrate** including the openings, and making the 2nd **oxide layer** remain as element sepn. films in only the element sepn. regions and (e) forming a **gate oxide film** and a **top** gate electrode on the residual mono-Si, and forming **source**/drain **regions** in the residual mono-**Si**. The insulating **film** is Si02.

USE/ADVANTAGE - Used in the mfr. of **Double Gated** (**MOS**) Thin Film Transistors (DGTFT). Noise resistance is enhanced. Sepn. between devices can be reduced, allowing higher integration.

mp

1b,c,d,f/2

43/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008584030
WPI Acc No: 1991-088062/199113
XRAM Acc No: C91-037412
XRPX Acc No: N91-068084
MOSFET with conductivity modulation - uses Schottky diode as collector resulting in faster turn-off and less danger of latch-up
Patent Assignee: FUJI ELECTRIC MFG CO LTD (FJIE); FUJI ELECTRIC CO LTD (FJIE)
Inventor: SAKURAI K
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4026121	A	19910321	DE 4026121	A	19900817	199113	B
JP 3155677	A	19910703	JP 9053085	A	19900305	199133	
US 5273917	A	19931228	US 90565370	A	19900810	199401	
			US 92815761	A	19920102		

Priority Applications (No Type Date): JP 9053085 A 19900305; JP 89213968 A 19890819
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5273917	A		9	H01L-021/265	Div ex application US 90565370

Abstract (Basic): DE 4026121 A

The transistor consists of a high resitivity n-type region (2) which has on one surface a metal electrode forming a Schottky barrier (10) and on the ohter surface a p-type base-region (3). The Base-region has a p(+)type well formed in it (5) inside which n(+) type regions (4) are formed. A gate electrode (7) on **top** of the **gate-oxide layer** (6) defines a channel-region (30) between the diffusions (4) and the **substrate** region (2). An emitter electrode (8) is formed of metal which connects to both the n+-and p(+)-type regions (4,5). A structure with the opposite conductivity types is also claimed.

Modifications claimed of this structure are: (1) the addn. of a second, higher doped n-region between the high resistivity region (2) and the Schottky barrier. (2) the addn. of discrete p-type collector regions adjacent to the metal electrode (10). The high resistivity region pref. has a doping level of 10 power 14-5 x 10 power 15 cm (-3).

USE/ADVANTAGE - The transistor shows less danger of latch-up because, compared with the current high performance transistors one of the transistor regions, which included the p-type collector region, is formed with the Schottky barrier which features a lower gain. The transistor also switches off faster, in that the electrons left in the n-type region (2) at switch-off is drawn out by the Schottky barrier contact instead of being left to recombine. ((9pp Dwg.No.5/7

Abstract (Equivalent): US 5273917 A

Conductive modulation **MOSFET** is produced by implanting ions into an FZ **semiconductor** wafer and bonding this via a **silicon dioxide film** to a CZ wafer. A field **oxide layer** is applied to the FZ surface with a well with high impurity concn. on part of the FZ surface adjacent to the

gate oxide film.

Polycrystalline **silicon film** above the gate forms the electrode. Using the **gate** as a mask, **second** type impurities are diffused into the FZ wafer surface including the well. Finally a **source region** with high impurity concn. is formed in the base region.

ADVANTAGE - The device provides enhanced switching speeds with a reduced risk of latching due to stray currents.

Dwg.1/7

43/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007956601
WPI Acc No: 1989-221713/198931
XRAM Acc No: C89-098443
XRPX Acc No: N89-169180
Depletion type DD-**MOSFET** device prodn. - by highly reproducible technique allowing threshold voltage to be controlled and adjusted easily
Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW)
Inventor: AKIYAMA S; NOBE T; SUZUMURA M; AKIYAMAMA S
Number of Countries: 005 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3901369	A	19890727	DE 3901369	A	19890118	198931	B
GB 2214351	A	19890831	GB 89297	A	19890106	198935	
JP 1183856	A	19890721	JP 888993	A	19880118	198935	
US 4902636	A	19900220	US 89294787	A	19890109	199014	
GB 2214351	B	19910220				199108	
US 5055895	A	19911008	US 89433979	A	19891109	199143	
CA 1306313	C	19920811	CA 587805	A	19890109	199238	

Priority Applications (No Type Date): JP 888993 A 19880118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3901369	A		7		
US 4902636	A		6		
CA 1306313	C			H01L-029/78	

Abstract (Basic): DE 3901369 A
In the prodn. of a **DMOSFET** device of the depletion type, the following stages are used: (1) forming an insulating **film** on a **Si** wafer; (2) forming window(s) in the **top** of the insulating **film**; (3) diffusing a first impurity of the opposite conductivity type to the wafer through this window; (4) covering the window with another insulating film; (5) forming another window in the insulating film, which is bounded by the outer edge of the first window; (6) diffusing a second impurity of the opposite conductivity type to the wafer and sequentially diffusing an impurity of the same conductivity type as the wafer through the second window to form channel zone, trough zone and source zone of the opposite conductivity type to the wafer; and (7) forming gate electrode using a **gate oxide** on **top** of the channel zone; and (8) forming source and drain electrodes. The novel features are that, after removing the insulating film in a zone bounded by the trough zone, masks are applied to the top of the source electrodes, which are connected to the trough and source zones; and ion implantation is carried out with an impurity of the same conductivity type as the wafer only in a relatively small zone, which includes the channel zone.
USE/ADVANTAGE - The threshold voltage can be controlled and adjusted easily, the process is highly reproducible and the device has high dielectric strength.
1H/2
Abstract (Equivalent): GB 2214351 B
A method for manufacturing a depletion type DMOSFET device

comprising the steps of forming an insulating **layer** on a **silicon substrate**, forming at least an opening in top surface of said insulating layer, carrying out a first diffusion of impurity material of a different conductivity type from said **substrate** through said opening, covering said opening with further insulating layer, forming a further opening in the insulating layer at its part externally adjacent said **opening**, carrying out a **second** diffusion of the impurity material that is different from the conductivity type of the **substrate** through said further opening to form a well region, sequentially carrying out through the further opening a further diffusion of an impurity material of the same conductivity type as the **substrate** to form **source regions** in surface **area** of the well region of the different conductivity type from the **substrate**, with channel regions formed at portions of the well **region** between the **source regions** and the **substrate** surrounding the well region, removing the insulating layer on said well and **source regions**, forming gate electrodes on said channel regions of said well region with a **gate oxide layer** interpose, and forming a source electrode on central part of said well region and adjacent part of said **source region** and a drain electrode on reverse side of the **substrate**, wherein said removal of the insulating layer oh the well and **source regions** is carried out to remove the insulating layer also on a part of the **substrate** outwardly adjacent the well region while leaving the insulating layer surrounding the wall region and said adjacent **substrate** part, a mask is provided on an area including said central part of the well region and adjacent part of the **source region** oh which said **source** electrode is to be formed, an ion-implantation of the impurity of the same conductivity type as the **substrate** is carried out in said well and **source regions** including said channel region and said s

Abstract (Equivalent): US 5055895 A

Depletion type **DMOSFET** (doube diffused **metal-oxide-semiconductor** field defect transistor) device comprises; (1) a Si wafer including a reverse size zone with high impurity concn. reverse size zon

US 4902636 A

A depletion type **DMOSFET** device is made by forming a first insulating **layer** (I) on a **silicon** wafer. At least a first opening is formed in a top surface of (I). A first diffusion is effected of an impurity material (II), of a different conductivity type from the wafer, through the first opening. The first opening is covered with a second insulating layer. A **second opening** is formed in the insulating layer with a part outwardly adjacent the first **opening**. A **second** diffusion is effected of (II) through the **second opening**. A third diffusion is effected of an impurity material of the same conductivity type as the wafer, through a third opening to form well and **source regions**. The insulating layer on the well and **source regions** is removed by at least 5 microns from the outer peripheral edges of the third opening. A mask is on an area including the central part of the well region, and an adjacent part of the **source region** on which the **source** electrode is formed. An ion-implantation is effected of an impurity in the well and **source regions** including the channel region and the wafer part adjacent the well region from which the insulating layer has been removed, except for the area on which the mask is provided. The mask is then removed. Gate electrodes are formed

with a **gate oxide layer** on the channel region of the well **region**. A **source** electrode is formed on a central part of the well region and adjacent parts of the **source regions** and a drain electrode on the reverse side of the wafer.

ADVANTAGE - **DMOSFET** is easy to control and set the threshold voltage, is high in process reproducibility and freedom, and shows high breakdown voltage characteristics. (6pp)c

43/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007151689
WPI Acc No: 1987-151686/198722
XRAM Acc No: C87-063294
XRPX Acc No: N87-113788
CMOS integrated circuit - using p-doped polycide gate-electrode
Patent Assignee: SIEMENS AG (SIEI)
Inventor: GIERISCH H; NEPPL F
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 224199	A	19870603	EP 86116077	A	19861120	198722	B
JP 62131561	A	19870613	JP 86279518	A	19861121	198729	
US 4782033	A	19881101	US 86928893	A	19861110	198846	
EP 224199	B	19900131				199005	
DE 3668727	G	19900308				199011	
KR 9502276	B1	19950315	KR 869940	A	19861125	199706	

Priority Applications (No Type Date): DE 3541940 A 19851127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 224199	A	G	7		
US 4782033	A		6		
EP 224199	B	G			
KR 9502276	B1			H01L-027/092	

Abstract (Basic): EP 224199 A
The gate-electrodes of both types of transistors in the **CMOS** -device consist of a double-**layer** of polycrystalline **silicon** and metal-silicide. The **polysilicon layer** (4), pref. 100nm thick, is deposited undoped on the 20nm thick **gate-oxide layer** (2) and field-**oxide** (3) on the **substrate** (1). On **top** of this polysi **layer** a layer of metal-silicide (5), pref. Ta-silicide 200nm thick, is deposited. Then the entire surface is covered with a deposited **layer** (6), pref. **Si-oxide** deposited by thermal decomposition of tetra-ethyl-ortho-silicate and 100nm thick. This layer masks against the later following P-implantation used to form **source**- and drain-**regions**. Boron-ions are (7) implanted, pref. 5 x 10 power (15) cm-2 at 40 KeV, through the **oxide** into the silicide-**layer**. During a treatment at a high temp. this B diffuses into the polysi-layer. The double layer also recrystallises. Using a photo-resist process the gate-electrode is now formed. The device is then completed in the standard way.

USE/ADVANTAGE - The use of a p+-doped polycide gate-electrode achieves a favourable device-threshold without extra channel-doping. This reduces the punch through effect in the p-channel transistor and hot electron effects in the n-channel devices. The process makes it possible to use a simple modification of the standard process to produce this p+-doped polysi gate-electrode without the danger of penetration of the **gate-oxide** by the B-dopant during subsequent processing.

Abstract (Equivalent): EP 224199 B
Process for producing highly integrated circuits (**CMOS**)

containing p- and n-channel **MOS** transistors, in which process the **gate** electrodes consist of **double** layers of high-melting metal sili-cides and polycrystalline silicon, and the doping of the polycrystalline **silicon layer** takes place by outdiffusion from the metal silicide layer, and in which process production of the active transistor regions, the channel **regions**, the **source** /drain **regions** and the gate electrodes, as well as the production of the conductor track planes, is carried out in accordance with known process steps of **semiconductor** technology, wherein during the course of the process after the production of the **gate oxide** (2) in the **gate** region of the p- and n-channel transistors, a) the layer (4) consisting of undoped polycrystalline silicon is deposited on the **substrate** surface provided with the **gate oxide layer** (2), b) the metal silicide layer (5) is applied thereon, c) the double layer (4, 5) of polycrystalline silicon and metal silicide is provided with a layer (6) masking the later source/ drain implantation for the n-channel **MOS** transistors and and preventing a redoping of the gate, d) boron atoms are introduced into the metal silicide layer (5) by means of whole-area ion implantation (7), e) a high-temperature treatment is carried out, an out-diffusion of the boron ions taking place from the metal silicide layer (5) into the polycrystalline **silicon layer** (4), and the double layer (4, 5) being crystallised and f) the double layer (4, 5) provided with the masking layer (6) is structured after carrying out a photoresist technique to form gate electrodes. (7pp)

Abstract (Equivalent): US 4782033 A

Highly integrated circuit contg. p- and n-channel **MOS** transistors is produced from a Si **substrate**, on which **gate** o **oxide** and field **oxide layers** are formed before deposition of undoped poly-**Si layer**. Refractory metal silicide later is then deposited and masking layer is provided to mask source/drain implantation to be formed. B ions are introduced into the refractory metal silicide layer by ion implantation over the entire surface and the b infiltrated material is subjected to a temp. sufficiently high to cause B ions to diffuse out of the silicide layer into the polycrystalline layer, while the **double** layer is crystallised. **Gate** electrodes are formed in the double layer, using the masking layer.

ADVANTAGE - B penetration which occurs under thermal stress and caused by the use of B-doped polycide gates is avoided

43/3,AB/13 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02248465
SEMICONDUCTOR DEVICE

PUB. NO.: 62-165365 [JP 62165365 A]
PUBLISHED: July 21, 1987 (19870721)
INVENTOR(s): OYA SHUICHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-006227 [JP 866227]
FILED: January 17, 1986 (19860117)
JOURNAL: Section: E, Section No. 570, Vol. 12, No. 3, Pg. 148, January 07, 1988 (19880107)

ABSTRACT

PURPOSE: To prevent oxidation and improve electrical characteristics of a device and improve the reliability by levelling the wiring by a method wherein a layer insulating film has a triple-layer structure composed of a **silicon oxide film**, a **silicon** nitride **film** and an impurity doped silica glass film laminated in this order from the lower layer to the upper layer.

CONSTITUTION: After a **gate silicon oxide film** 2 is made to grow on a P-type single crystal silicon **substrate** 1, a phosphorus doped polycrystalline **silicon film** 3 is made to grow on the film 2 and further a tungsten silicide film 4, as a high melting point metal silicide, is made to grow on the film 3. After that a **gate** electrode of a **double** -layer structure is formed by patterning. Then arsenic ions are implanted into the silicon **substrate** 1 as an N-type impurity to form **source** and drain **regions** 6 and 6. A **silicon oxide film** 7 is made to grow on the regions 6 and 6 and a **silicon** nitride **film** 8 is formed on the **oxide film** 7 and further a BPSG film 9 containing boron and phosphorus is formed on the film 8 to form a layer insulating film 10 of a triple-layer structure. the layer insulating film 10 is subjected to a heat treatment in a stream atmosphere and the BPSG film 9 which is the **top layer** is made to reflow to relieve its stepped parts.

47/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014393699
WPI Acc No: 2002-214402/200227
XRAM Acc No: C02-065585
XRPX Acc No: N02-164032
Formation of **metal oxide semiconductor field effect transistor** (**MOSFET**) for dynamic random access memory (DRAM) cell involves providing sacrificial layer to save portion of two **silicon oxide layer** during successive etching
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: HUANG J; TSAI C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6265274	B1	20010724	US 99431954	A	19991101	200227	B

Priority Applications (No Type Date): US 99431954 A 19991101
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6265274	B1		12	H01L-021/336	

Abstract (Basic): US 6265274 B1
Abstract (Basic):
NOVELTY - A **metal oxide semiconductor field effect transistor** is formed by providing two **silicon oxide layers** on **gate** and dielectric layer; providing sacrificial layer to save predetermined portion of the two **silicon oxide layers**; and performing successive etching to remove sacrificial **layer** on **top** of the **gate**, and the **two silicon oxide layers** on the protruding portion of the gate.
DETAILED DESCRIPTION - Formation of **metal oxide semiconductor field effect transistor** (**MOSFET**) on a wafer (30), comprising silicon **substrate** (12), and dielectric layer (14), involves forming a gate (16) on dielectric layer portion(s); forming a first **silicon oxide layer** (18) on the wafer, thus covering the gate; performing first ion implantation to form two doped areas (22) at two opposite sides of the gate used as lightly doped drains of the **MOS** transistor (38); forming a second **silicon oxide layer** (32) on the wafer, thus covering the first **silicon oxide layer**; forming sacrificial **layer** on the second **silicon oxide layer**; performing first etching to remove the sacrificial **layer** on **top** of the gate, causing the gate to protrude from the remaining sacrificial layer; performing a second etching process to remove the first and second **silicon oxide layers** on the protruding portion of the gate; removing the sacrificial **layers**; forming a **silicon** nitride **layer** on the wafer to cover the protruding portion of the gate and the remaining **silicon oxide layers**; performing a third anisotropic etching to remove the **silicon** nitride **layer** on **top** of the gate, thus forming a spacer (37); and performing a second ion implantation to form two doped areas on the **substrate** that are

used as source and drain of the **MOS** transistor.

USE - Forming **metal oxide semiconductor field effect transistor** (**MOSFET**) used as pass transistor of dynamic random access memory cell (claimed).

ADVANTAGE - The method provides a **substrate** surface that is not coarsened by the ion implantation process, thus no short-circuiting occur between gate and the a subsequent contact plug.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a **MOS** transistor formed using the above process.

Substrate (12)
Dielectric layer (14)
Gate (16)
Oxide layer (18, 32)
Doped areas (22)
Spacer (37)
MOS transistor (38)
pp; 12 DwgNo 14/15

47/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014349759
WPI Acc No: 2002-170462/200222
XRAM Acc No: C02-052572
XRPX Acc No: N02-129622
Dual-gate CMOS device production
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: SHIU S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 424303	A	20010301	TW 99110149	A	19990617	200222	B

Priority Applications (No Type Date): TW 99110149 A 19990617
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 424303	A		25	H01L-021/8238	

Abstract (Basic): TW 424303 A
Abstract (Basic):

NOVELTY - Production of a **dual-gate CMOS** device produces a smaller device formed by a simpler process.

DETAILED DESCRIPTION - A **dual-gate CMOS** device comprises an amorphous **silicon layer**. Production of the device comprises:

(a) forming isolation areas in the **semiconductor substrate**;

(b) forming a P-well and an N-well respectively isolated by the isolation areas;

(c) sequentially forming a **gate oxide** and a **polysilicon layer** on **top** of the P-well and N-well;

(d) forming a first dielectric on the **polysilicon layer**;

(e) forming a first photoresist layer on the first dielectric layer and etching the first dielectric and the **polysilicon layer** in which the **polysilicon layer** is used to define the N-type **gate** area of **dual-gate CMOS**;

(f) depositing an amorphous **silicon layer** on the **gate oxide** and the surface of the first dielectric layer and forming a second dielectric on the surface of the amorphous **silicon layer**;

(g) depositing a spin-on glass layer on the second dielectric layer;

(h) chemical mechanical polishing to etch the spin-on glass layer, the second dielectric and the amorphous **silicon layer** until the first dielectric is reached; and

(i) back etching to etch the partly raised amorphous silicon and etching the first and the second dielectric layers in which the local amorphous **silicon layer** is used to define the P-type **gate** area of the **dual-gate CMOS**.

ADVANTAGE - A small sized **semiconductor** device is obtained in a simpler manufacturing method.

pp; 25 DwgNo 1A/7

47/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013972443
WPI Acc No: 2001-456656/200149
Related WPI Acc No: 2000-022877; 2000-292378; 2000-646357; 2001-089790
XRAM Acc No: C01-138058
XRPX Acc No: N01-338407
Fabrication of flash electrically erasable programmable read only memory device having array of cells by employing **polysilicon** sidewall **spacer** as erase gate
Patent Assignee: CHANG M (CHAN-I)
Inventor: CHANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6261907	B1	20010717	US 9860673	A	19980415	200149	B
			US 99453395	A	19991203		

Priority Applications (No Type Date): US 9860673 A 19980415; US 99453395 A 19991203
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6261907	B1		16	H01L-021/336	Div ex application US 9860673 Div ex patent US 6043530

Abstract (Basic): US 6261907 B1
Abstract (Basic):
NOVELTY - Fabrication of flash electrically erasable programmable read only memory (EEPROM) device having an array of cells involves depositing and etching back an erase-gate **polysilicon layer** to form **polysilicon** sidewall **spacers** (107) having a thickness of 0.1-0.3 mum on the device.
DETAILED DESCRIPTION - Fabrication of flash EEPROM device having an array of cells includes providing peripheral P-**metal oxide semiconductor** (**PMOS**) and **NMOS** transistors and a flash EEPROM device on a silicon **substrate** by providing a partially processed **semiconductor** wafer including a floating **gate oxide** (103), a first **polysilicon layer** on the **gate oxide**, a **second polysilicon layer** on the **gate oxide** with an **interpolysilicon** dielectric **layer** in-between, and an **oxide** cap (601) on **top** of the second **polysilicon layer**.
The oxide cap and the second **polysilicon layer** are patterned and etched so that portion of the **polysilicon layer** forms a control gate structure presenting sidewalls.
Dielectric spacers (106) having a thickness of 350-650Angstrom are formed on the sidewalls of the gate structure, on peripheral transistors.
The first **polysilicon layer** is etched so that its portion forms a floating **gate** structure, using the **oxide** cap and the dielectric spacers as hard masks for etching. Boron is implanted to shift an erase gate threshold voltage to IV.
A portion of the floating gate is stripped on the silicon **substrate**. An erase **gate oxide** is grown with a thickness of 50-250Angstrom. A poly tunnel oxide (109) is grown on

sidewalls of the floating gate structure during the growing of the erase **gate oxide**. An erase-**gate polysilicon layer** is deposited and etched to form **polysilicon** sidewall **spacers** with a thickness of 0.1-0.3 mum on the device.

Polysilicon contact pads are formed with photolithography masks during deposition and etching back. Layer of the spacers are stripped on one side of the device. A field oxide is etched along source lines. N+ arsenic is implanted for the **NMOS** transistor as well as array cells. The spacers of the transistors are stripped followed by N- implant. P+ boron is implanted for the **PMOS** transistor.

USE - For fabricating flash EEPROM device having array of cells.

ADVANTAGE - The invention provides a memory device that requires low currents for both programs and erase operations, thus suitable for low power supply (Vcc), low power, high density flash memory applications.

DESCRIPTION OF DRAWING(S) - The figures show sectional views of an array cell and peripheral transistors.

Floating gate (103)
Dielectric layer (106)
Polysilicon sidewall **spacer** (107)
Poly tunnel oxide (109)
Oxide cap (601)
pp; 16 DwgNo 6/6

47/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013788479
WPI Acc No: 2001-272690/200128
XRAM Acc No: C01-082636
XRPX Acc No: N01-194707

Manufacture of **semiconductor** device, e.g. **metal-oxide semiconductor** transistor, by using salicide process for removing residue on **substrate** surfaces

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: BESSER P R; CHAN S S; HUI A T; NGO M V

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6204136	B1	20010320	US 99386466	A	19990831	200128	B

Priority Applications (No Type Date): US 99386466 A 19990831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6204136	B1		8	H01L-021/336	

Abstract (Basic): US 6204136 B1
Abstract (Basic):

NOVELTY - A **semiconductor** device is made by using salicide process where residue on **substrate** surfaces resulting from reactive plasma etching for sidewall spacer formation is removed prior to salicide processing.

DETAILED DESCRIPTION - Manufacture of a **semiconductor** device by providing a **semiconductor substrate** having a surface. A thin gate insulator layer (5) is formed in contact with the **substrate** surface. A gate electrode is formed on a portion of the gate insulator layer. The **gate** electrode comprises **two** opposing side surfaces and a **top** surface. A blanket **layer** of an insulative material is formed on the exposed portions of the thin gate insulator layer on the **substrate** surface and on the two opposing side surfaces and top surface of the gate electrode. The blanket layer of insulative material and underlying portions of the thin gate insulator layer from the **substrate** surface, and the blanket layer of insulative material from the top surface of the gate electrode are removed by anisotropically etching, thus forming an insulative sidewall spacer (9') on each opposing side surface of the gate electrode and each exposing portion of the **substrate** surface adjacent the sidewall spacers. The residue and/or contaminants resulting from anisotropically etching of the exposed portions of **substrate** surface are removed.

USE - For manufacturing **semiconductor** devices, e.g. **metal-oxide semiconductor** (**MOS**) or complementary **MOS** transistors.

ADVANTAGE - The invention enables formation of reliable, defect-free, low junction leakage, sub-micron-dimensioned **MOS** transistors and **CMOS** devices at rates consistent with the requirements at manufacturing throughput, and is fully compatible with conventional process flow for automated manufacture of high-density integration **semiconductor** devices.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional

schematic view of a **MOS** transistor.
Thin gate insulator layer (5)
Insulative sidewall spacer (9')
Electrically conductive silicide (11, 12, 12')
pp; 8 DwgNo 3/3

47/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013370523
WPI Acc No: 2000-542462/200049
XRAM Acc No: C00-161391
XRPX Acc No: N00-401186
Termination structure for **high voltage** transistors comprises a conductive layer atop an overlaying insulation layer over the field insulation material **layer** and **polysilicon** field plates on top of the regions of impurities
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: KINZER D M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6100572	A	20000808	US 9613761	A	19960320	200049 B
			US 97822398	A	19970320	

Priority Applications (No Type Date): US 9613761 P 19960320; US 97822398 A 19970320
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6100572	A		9	H01L-023/58	Provisional application US 9613761

Abstract (Basic): US 6100572 A
Abstract (Basic):
NOVELTY - A termination structure comprises a conductive layer atop an overlaying insulation layer over the field insulation material **layer** and **polysilicon** field plates formed over the field insulation material **layer** on **top** of the region(s) of impurities adjacent the lightly doped resurf layer on the **substrate**; and amorphous **silicon layer** on the two electrodes and the overlaying insulation layer.
DETAILED DESCRIPTION - The termination structure for a **semiconductor** device having an active region and a silicon **substrate** of a first conductivity type comprises a lightly doped resurf layer (30) of a second conductivity type formed on the **substrate** to a given and constant depth and in contact with the active region; region(s) of impurities of the first conductivity type formed adjacent the resurf layer and has a depth equal to the given depth; a layer of field insulation material (31) on top of the first portion of the region(s) of impurities (32); two polysilicon field plates (33b, 33c), the first is on top of the region(s) of impurities not covered by the layer of field insulation material and extends over part of the layer of field insulation material, the second is over the layer of field insulation material and partly over an active junction of the active region; diffused regions on the surface regions of the silicon **substrate** located at the end of the **substrate**; an overlaying insulation layer formed over the layer of field insulation material and two polysilicon field plates; a conductive layer atop the overlaying insulation layer, part is removed to define a first electrode which contacts the second polysilicon field plates; and an amorphous **silicon layer** (80) atop the two electrodes and atop the overlaying insulation layer.
USE - For **high voltage** (600 **volts** or higher)

metal oxide semiconductor (**MOS**) **gate** devices or **high voltage** transistors.

ADVANTAGE - The combined resurf region and semi-insulating layer form a **high voltage** termination structure.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-section view of the termination structure.

P-type (21)
N-type (22)
Lightly doped resurf layer (30)
Layer of field insulation material (31)
Region of impurities (32)
Polysilicon field plates (33b, 33c)
Low temperature **oxide layer** (60)
Amorphous **silicon layer** (80)
pp; 9 DwgNo 5/6

47/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012470381
WPI Acc No: 1999-276489/199923
XRAM Acc No: C99-081135
XRPX Acc No: N99-207233
Local oxidation of silicon (LOCOS) for fabrication of field oxide isolation regions - using **silicon** nitride **spacers** for a smooth surface and improved step coverage
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: HSU S; HUANG Y; TSAI C; WU J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5895257	A	19990420	US 96691288	A	19960801	199923	B

Priority Applications (No Type Date): US 96691288 A 19960801
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5895257	A		7	H01L-021/76	

Abstract (Basic): US 5895257 A

NOVELTY - **Silicon** nitride sidewall **spacers** are formed on the sidewall of the field **oxide** isolation regions, these **spacers** cover recesses formed by preferential etching after using retrograde well technology for well formation, and provide a smoother surface giving improved step coverage in subsequent processing.

DETAILED DESCRIPTION - Method of forming field oxide isolation comprising; (a) Providing an integrated circuit **substrate** with an isolation region on its first surface. (b) Forming in sequence, pad **oxide**, first **layer** of **silicon** nitride, isolation pattern in the nitride by removing the nitride directly over the isolation region. (c) Forming field oxide by oxidation of the isolation region using the patterned nitride as a mask. (d) Removing the first nitride **layer** and pad **oxide** by wet isotropic etching to form recesses in the sidewalls of the field oxide. (e) Forming sacrificial oxide over all. (f) Forming device well regions in the **substrate** by ion implantation. (g) Formin g second **silicon** nitride **layer** covering the **top** and sidewalls of the field oxide. (h) Removing all the second nitride layer except that over the field oxide sidewalls by dry anisotropic etching to form nitride sidewall spacers covering the recesses. (i) removing the sacrificial **oxide** and forming **gate oxide**.

USE - **Metal oxide semiconductor field effect transistors** (**MOSFETs**)

ADVANTAGE - The method gives a smoother surface and improved step coverage improving the reliability of subsequent processes.

DESCRIPTION OF DRAWING(S) - The drawings show steps in the process including; (10) **substrate**, (12) field oxide isolation region, (16) active regions, (20) pad oxide, (22) sacrificial oxide, (24) first silicon nitride, (27) **silicon** nitride **spacers** from **second** nitride, (28) **gate oxide**.

Dwg.6,7,8/9

47/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011223567
WPI Acc No: 1997-201492/199718
XRAM Acc No: C97-064398
XRPX Acc No: N97-166598
Sub-half micron channel length **MOSFET** device - improves circuit performance by reductions in junction capacitances
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: JIN-YUAN L; MONG-SONG L; LEE J; LIANG M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5614430	A	19970325	US 96613652	A	19960311	199718	B
SG 45504	A1	19980116	SG 9610762	A	19960919	199812	

Priority Applications (No Type Date): US 96613652 A 19960311
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5614430	A		13	H01L-021/762	
SG 45504	A1			H01L-029/00	

Abstract (Basic): US 5614430 A
Fabricating a **MOSFET** device on a **semiconductor substrate** comprises:
forming a shallow trench in the **substrate**;
depositing a first insulator layer on the **substrate** and completely filling the shallow trench;
removing the first insulator layer from all areas of the **substrate** except from the trench;
depositing a second insulator layer on the **substrate** including on the first insulator layer in the shallow trench;
opening a region in the second insulator layer to an area of the **substrate** to be used for a gate region;
ion-implanting a first dopant of a first conductivity type into the opened region in the insulator layer;
growing a **gate oxide** on the region of the **substrate** exposed in the opened region of the second insulator layer;
depositing a first **polysilicon layer** on the surface of the second insulator layer and on sides of the opened region in the second insulator **layer** creating a **polysilicon** side wall, and on the surface of the **gate oxide** exposed in the opened region of the second insulator layer;
ion implanting a second dopant of the first conductivity type through the first **polysilicon layer**, through the **gate oxide**, and into the **substrate** in the opened region of the second insulator layer not covered by the polysilicon side wall;
depositing a second **polysilicon layer** on the first **polysilicon layer**;
ion implanting a third dopant of the second conductivity type into the second **polysilicon layer**;
removing the second **polysilicon layer** and the first **polysilicon layer** from the **top** surface of the second insulator **layer** to form a **polysilicon gate** structure

of the **second polysilicon layer**, and the first **polysilicon layer** in the opened region of the second insulator layer;

removing the second insulator layer;

ion implanting a fourth dopant of the second conductivity type into the **substrate** not covered by the polysilicon gate structure;

depositing a third insulator layer on the **substrate** and on the polysilicon gate structure;

anisotropically etching the third insulator layer to form an insulator spacer on sides of the polysilicon gate structure;

ion implanting a fifth dopant of the second conductivity type into the **substrate** not covered by the polysilicon gate structure or by the insulator spacer;

depositing a fourth insulator layer on the **substrate**, including depositing on the polysilicon gate structure;

opening a contact hole in the fourth insulator layer to a region in the **substrate**;

depositing a metal **layer** on the **top** surface of the fourth insulator layer and on the surface of the region on the **substrate** exposed in the contact hole; and

patterning the metal layer to form a metal contact structure to the region on the **substrate**.

USE - Mfr. of sub-half micron channel length **MOSFET** device.

ADVANTAGE - Reduced exposure to source and drain leakage currents arising from junction depletion punch-through phenomena, with only a minimal increase in parasitic capacitance.

Dwg.9/13

47/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010264041
WPI Acc No: 1995-165296/199522
XRAM Acc No: C95-076403
XRPX Acc No: N95-129813
Semiconductor memory device manufacturing method - by forming **silicon@ film** to cover gate insulating film which hides whole surface of **second** set of **gate** electrodes
Patent Assignee: NEC CORP (NIDE)
Inventor: TASAKA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7086437	A	19950331	JP 93252234	A	19930914	199522	B
US 5490106	A	19960206	US 94305163	A	19940913	199612	

Priority Applications (No Type Date): JP 93252234 A 19930914
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7086437	A		7	H01L-021/8246	
US 5490106	A		24	G11C-017/00	

Abstract (Basic): JP 7086437 A

The manufacturing method is applied to a P type silicon **substrate** (1) on the main field of which a first set of gate electrodes (2) is installed. A **second** set of **gate** electrodes (4) is mounted on an isolation **oxide film** (3) **layered** on the **substrate**. These gate electrodes are positioned between the first set of **gate** electrodes. A gate **oxide film** (5) is formed such that it covers the whole surface of the **second** set of **gate** electrodes. A **Si film** (6) is **layered** on the gate insulating film. Then, a source domain (7a) and a drain domain (7b) are formed. The above processes result in the formation of a reverse multigate TFT **MOSFET**. Then, ion implantation is carried out to perform information write-in.

ADVANTAGE - Improves pouring accuracy, reliability and yield of device. Avoids channel offset between gates. Realizes LSI.

Dwg.14/14

Abstract (Equivalent): US 5490106 A

A **semiconductor** read only memory device fabricated on a **semiconductor** bulk **substrate**, and having a number of memory cell blocks each including series combinations of memory cells and switching transistors, each of the memory cell blocks comprising:

a) a number of conductive strips including elongated impurity regions at intervals in surface portions of the **semiconductor** bulk **substrate** and **semiconductor** strips in grooves between the elongated impurity regions, the number of conductive strips having respective top surfaces, and providing gate electrodes of the series combinations of memory cells and switching transistors,

b) a number of first insulating films in the grooves for electrically isolating the number of conductive strips from one another,

c) a gate insulating **layer** covering the **top** surfaces of

the number of conductive strips, and

d) a number of **semiconductor** layers extending over the gate insulating layer and spaced apart from one another, the number of **semiconductor** layers being respectively associated with the series combinations of memory cells and switching transistors for providing channel regions of the memory cells and channel regions of the switching transistors.

Dwg.1/12

47/3,AB/10 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03742732
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 04-107832 [JP 4107832 A]
PUBLISHED: April 09, 1992 (19920409)
INVENTOR(s): ARUBERUTO O ADAN
HOTTA MASAYOSHI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-227068 [JP 90227068]
FILED: August 27, 1990 (19900827)
JOURNAL: Section: E, Section No. 1240, Vol. 16, No. 347, Pg. 130, July 27, 1992 (19920727)

ABSTRACT

PURPOSE: To be able to insulate the transistor from the **substrate** using the effect of shielding the lower part of the gate electrode and thereby improve transistor properties by using a **double gate** structure based on selective epitaxial growth in the crosswise direction.

CONSTITUTION: A first **oxide film** 2 is formed on a silicon **substrate** 1 and a polysilicon layer 3 is **layered** on **top** as the lower portion of the gate electrode and thermally oxidized. Next, the polysilicon layer 3 and the SiO(sub 2) film 2 are patterned and the region R of the silicon **substrate** 1 is exposed. Epitaxial tech nology is applied across the entire surface to grow a single crystal **silicon layer** 5. This **layer** is etched and a CVD **oxide layer** 6 is used as a dielectric isolation film to leave region R. A **gate oxide film** 7 is formed on the residual epitaxial **silicon film** 5a and a contact window 8 is created between the upper portion gate polysilicon electrodes as a stacked contact. After layering the polysilicon layer, which constitutes the upper portion electrode, and etching, the upper portion electrodes 14, 9 are left only on the single crystal **silicon film** 5a. The insulating later 15 is applied to the entire surface and then the metal layer 17 is applied.

47/3,AB/11 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01944070
MANUFACTURE OF CHARGE TRANSFER DEVICE

PUB. NO.: 61-158170 [JP 61158170 A]
PUBLISHED: July 17, 1986 (19860717)
INVENTOR(s): OTSU KOJI
SAITO KATSUYUKI
SATO MAKI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-280075 [JP 84280075]
FILED: December 28, 1984 (19841228)
JOURNAL: Section: E, Section No. 460, Vol. 10, No. 359, Pg. 164, December 03, 1986 (19861203)

ABSTRACT

PURPOSE: To reduce the thickness of an insulating film and thereby to realize a microstructure output **MOS-FET** by a method wherein the gate insulating film for the **MOS-FET** is composed only of an SiO(sub 2) layer that is formed simultaneously with the oxidation of the surface of first **layer** polycrystalline **silicon** electrodes at a CCD forming location.

CONSTITUTION: An SiO(sub 2) layer 5 and SiN layer 6 are formed on a **semiconductor substrate** 1 and then, in a CCD forming location 2, first alyer polycrystalline silicon electrodes 7 are formed on the SiN layer 6 to serve as charge transfer electrodes. The SiO(sub 2) layer 5 and SiN alyer 6 are subjected to selective removal, only from a location 4 to develop into a gate in a output **MOS-FET** forming location 3. Oxidation is accomplished for the formation of an **oxide film** 8a on **top** of the first **layer** polycrystalline **silicon** electrodes 7 and, simultaneously, of a **gate oxide film** 8b in the output **MOS-FET** forming location 3. Next, a second alyer polycrystalline silicon is formed, and then subjected to patterning for the formation of a **second** alyer polycrystalline silicon **gate** electrode 9 in the output **MOS-FET** forming lcoation 3 and, simultaneously, of a plurality of second **layer** polycrystalline **silicon** electrodes 10 to serve as charge transfer electrodes between the first **layer** polycrystalline **silicon** electrodes 7 in the CCD forming location 2.

49/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014432688
WPI Acc No: 2002-253391/200230
Related WPI Acc No: 2001-353697; 2002-178841
XRAM Acc No: C02-075803
XRPX Acc No: N02-195500
Fabrication of integrated circuit device on **substrate** comprising **MOS** transistors and other components involves forming self-aligned contact windows to interconnect conductor columns and gate electrode layer to other components
Patent Assignee: MOSEL VITELIC INC (MOSE-N)
Inventor: NI C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6284578	B1	20010904	US 2000534699	A	20000324	200230	B

Priority Applications (No Type Date): TW 99104775 A 19990326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6284578	B1		11	H01L-021/338	

Abstract (Basic): US 6284578 B1
Abstract (Basic):
NOVELTY - Fabricating integrated circuit (IC) device on **substrate** comprises forming **dual gate** electrodes; forming raised source and raised drain; forming self-aligned silicide layers on conductor columns of gate electrode layers; forming self-aligned contact windows; and interconnecting conductor columns and **second gate** electrode layer to other IC components via the contact windows.

DETAILED DESCRIPTION - Fabricating an integrated circuit (IC) device on a **substrate** (10) comprising **metal oxide semiconductor** (**MOS**) transistors and other IC components involves forming isolation regions (12) on the **substrate** to separate active regions. Doped wells (20) are formed in the **substrate**. A first gate structure is formed on one of the active regions and a **second gate** structure is formed on one of the isolation regions adjacent the active region. Each gate structure comprises a gate electrode layer (16') of a first conductor material and a first dielectric layer. The **second gate** structure has a larger surface area than the first gate structure.

A second dielectric layer (24) is formed on the portions of the **substrate** other than those portions covered by the first and **second gate** structures. A mask layer is formed on the **second gate** structure and on the portions of the second dielectric layer other than those portions of the second dielectric layer adjacent to the first gate structure. The portions of the second dielectric layer adjacent the first gate structure are removed to form trenches next to the first gate structure. The mask layer is removed.

A second conductor material is deposited in the trenches to form conductor columns (28'). The first dielectric layers of the gate structures are removed. The gate electrode layers of the gate structures are doped with a second dopant to form the **dual gate** electrodes. A raised source electrode (38a) and a raised

drain electrode (38b) are formed.

Self-aligned silicide layers (30) are formed on the conductor columns and the gate electrode layers. A third dielectric **layer** is formed on **top** of the gate electrode layers to cover the gate electrode layer of the **second gate** structure partially and to form the self-aligned contact windows.

The conductor columns and the **second gate** electrode layer are interconnected to other transistors and other IC components by self-aligned window contacts.

USE - For fabricating an IC device on a **substrate**, particularly for fabricating **MOS** transistors having **dual gate** electrodes and self-aligned contact windows for interconnects.

ADVANTAGE - The invention is more compatible with deep sub-micron **semiconductor** processes than the conventional art for forming interconnected **semiconductor** transistors. The fabricated IC device can be operated at a lower voltage and has lower power consumption than conventional IC devices because the transistors of the new IC device have lower threshold voltages. The invention reduces planarizing difficulties during device fabrication so that it is easier to create multilayer, multi-metallization devices.

DESCRIPTION OF DRAWING(S) - The figure shows an IC device of the invention after formation of the interconnects at the self-aligned contact windows.

Substrate (10)
Isolation regions (12)
Gate oxide layer (14)
Gate electrode layer (16')
Doped wells (20)
Etch-stop layer (22)
Second dielectric layer (24)
Conductor columns (28')
Self-aligned silicide layers (30)
Raised source electrode (38a)
Raised drain electrode (38b)
pp; 11 DwgNo 6/6

49/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014358140
WPI Acc No: 2002-178841/200223
Related WPI Acc No: 2001-353697
XRAM Acc No: C02-055347
XRPX Acc No: N02-135997
Fabrication of integrated circuit device by forming raised source and drain electrodes, forming self-aligned silicide layers and interconnecting conductor columns, gate electrode layer, transistors and integrated circuit
Patent Assignee: MOSEL VITELIC INC (MOSE-N)
Inventor: NI C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010049165	A1	20011206	US 2000534699	A	20000324	200223 B
			US 2001896205	A	20010628	

Priority Applications (No Type Date): TW 99104775 A 19990326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010049165	A1		13	H01L-029/00	Div ex application US 2000534699

Abstract (Basic): US 20010049165 A1
Abstract (Basic):
NOVELTY - An integrated circuit (IC) device is made by forming raised source and drain electrodes; forming a self-aligned silicide layers on conductor columns and gate electrode layers; forming a dielectric layer to form self-aligned contact windows; and interconnecting the conductor columns and the **second gate** electrode layer to other transistors and IC components by contact windows.

DETAILED DESCRIPTION - Fabrication of an integrated circuit (IC) device on a **substrate** (10) comprises

(a) forming isolation regions (12) on the **substrate** to separate the active regions (11);

(b) doping the **substrate** to form doped wells (20);

(c) forming a first gate structure (13) on the active region(s) and a **second gate** structure on the isolation region(s) adjacent to the active region;

(d) forming a second dielectric layer on the portions on the **substrate** other than those portions covered by the first and **second gate** structures;

(e) forming a mask layer on the **second gate** structure and on the portions of the second dielectric layer other than those portions of the second dielectric layer adjacent to the first gate structure;

(f) removing the mask layer;

(g) depositing a second conductor material in the trenches to form conductor columns;

(h) removing the first dielectric layers of the first and **second gate** structures;

(i) doping the gate electrode layers of the first and **second**

gate structures with a **second** dopant to form the **dual gate** electrodes;

(j) forming raised source electrode and raised drain electrode;

(k) forming a self-aligned silicide layers on the conductor columns and the gate electrode layers;

(l) forming a third dielectric **layer** on **top** of the gate electrode layers to cover the gate electrode layer of the first gate structure entirely, and the gate electrode layer of the **second gate** structure partially and to form the self-aligned contact windows; and

(m) interconnecting the conductor columns and the **second gate** electrode layer to other transistors and other IC components by self-aligned contact windows.

The **substrate** comprises **metal oxide semiconductor** transistors and other IC components, where each transistor has a raised source electrode, a raised drain electrode and **dual gate** electrodes, and is interconnected by self-aligned contact windows to other IC components. Each of the first and **second gate** structures comprises a gate electrode layer (15) of a first conductor material, and a first dielectric layer. The **second gate** structure has a larger surface area than the first gate structure.

USE - For fabricating an integrated circuit device (claimed) on a **substrate**.

ADVANTAGE - The inventive method is more compatible with deep submicron **semiconductor** processes than the conventional art for forming interconnected **semiconductor** transistors. It reduces planarizing difficulties during device fabrication, making it easier to create multilayer, multimetallization devices. The method produces an IC device that can be operated at a lower voltage and has a lower power consumption than conventional IC devices because the transistors of the new IC device generally have lower threshold voltages.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic, cross-sectional representation of the IC device after formation of the active regions, isolation regions and **two gate** electrode structures.

Substrate (10)
Active regions (11)
Isolation regions (12)
First gate structure (13)
Gate electrode layer (15)
Doped wells (20)
pp; 13 DwgNo 1/6

49/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012662442
WPI Acc No: 1999-468547/199939
XRAM Acc No: C99-137336
XRPX Acc No: N99-349869
Forming a T-gate in a metal **semiconductor field effect transistor** (MESFET) for high frequency operation
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: YOO H M; NGUYEN X
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5940697	A	19990817	US 97941126	A	19970930	199939	B
KR 99028699	A	19990415	KR 98512	A	19980112	200027	
KR 276649	B	20010201	KR 98512	A	19980112	200210	

Priority Applications (No Type Date): US 97941126 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5940697	A		5	H01L-021/338	
KR 99028699	A			H01L-029/80	
KR 276649	B			H01L-029/80	Previous Publ. patent KR 99028699

Abstract (Basic): US 5940697 A
Abstract (Basic):
NOVELTY - The gate is fabricated by a deposition over a directly applied photoresist mask and lift off of unwanted material process. The process does not need deposition and etching of a dielectric film for forming a gate recess, and plasma damage to the **substrate** resulting from the etch back process is eliminated.
DETAILED DESCRIPTION - Method of forming a T-gate in a metal **semiconductor field effect transistor** (MESFET) by; (a) Forming a gate defining photoresist mask directly on a gallium arsenide (GaAs) **substrate** and sputtering silicon dioxide. (b) Lifting off part of the **oxide layer** formed over the mask to leave an **oxide layer** which defines a gate opening of a first cross-section. (c) Depositing a T-gate masking photoresist over the **oxide layer** having a **top** defining an **opening** of a **second** cross-section to expose a region of the **oxide layer** surrounding the **gate** opening. (d) Etching a gate recess in the **substrate** surface through the gate opening, and depositing a metal layer over the T-gate masking layer and the gate opening. (e) Stripping the T-gate masking layer to lift off the metal over it to leave a T-gate having a gate width substantially equal to first cross-section area and a top width equal to the second cross-section area.
USE - Fabrication of MESFETs for high frequency operation.
ADVANTAGE - The lift off process is simple and does not need expensive plant and does not result in device damage.
DESCRIPTION OF DRAWING(S) - The drawing shows a T-gate structure including;
GaAs **substrate** (12)
silicon oxide (14)
T-gate (24)

49/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011714030
WPI Acc No: 1998-130940/199812
XRAM Acc No: C98-043346
XRPX Acc No: N98-103300
MOS transistors with extended drift regions for **high voltage** applications - including a short channel length and an extended drift region with low doping concentration providing very low on-resistance together with high breakdown voltage
Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)
Inventor: SODERBARG A; SVEDBERG P; SOEDERBERG A; SOEDERBARG A; SOEDERBAERG A
Number of Countries: 079 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9805076	A2	19980205	WO 97SE1223	A	19970704	199812	B
SE 9602881	A	19980127	SE 962881	A	19960726	199815	
AU 9737118	A	19980220	AU 9737118	A	19970704	199828	
TW 335513	A	19980701	TW 97110091	A	19970716	199846	
US 5844272	A	19981201	US 97900829	A	19970725	199904	
EP 958613	A2	19991124	EP 97933941	A	19970704	199954	
			WO 97SE1223	A	19970704		
CN 1231770	A	19991013	CN 97198189	A	19970704	200008	
SE 513283	C2	20000814	SE 962881	A	19960726	200047	
KR 2000029578	A	20000525	WO 97SE1223	A	19970704	200110	
			KR 99700637	A	19990126		
JP 2001502846	W	20010227	WO 97SE1223	A	19970704	200115	
			JP 98508732	A	19970704		
KR 311589	B	20011103	KR 99700637	A	19990126	200240	

Priority Applications (No Type Date): SE 962881 A 19960726
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9805076	A2	E	15	H01L-029/78	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW					
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
SE 9602881	A			H01L-029/78	
AU 9737118	A				Based on patent WO 9805076
TW 335513	A			H01L-021/283	
US 5844272	A			H01L-029/76	
EP 958613	A2	E		H01L-029/78	Based on patent WO 9805076
Designated States (Regional): DE ES FI FR GB IT NL SE					
CN 1231770	A			H01L-029/06	
SE 513283	C2			H01L-029/78	
KR 2000029578	A			H01L-029/78	Based on patent WO 9805076
JP 2001502846	W		18	H01L-029/78	Based on patent WO 9805076
KR 311589	B			H01L-029/78	Previous Publ. patent KR 2000029578

Abstract (Basic): WO 9805076 A

A device forming a **high voltage MOS** transistor comprises: (a) a **substrate** (20) with an n-doped **semiconductor** layer (21); (b) first n+-doped drain area (23); (c) a p-doped body (22) containing a second n+-doped region (24) and first p+-doped region (25) forming a source area; (d) an insulating **gate oxide layer** (26), having on **top** a **semiconductor layer**, which together with the insulating **gate oxide** forms an extended **gate** layer; and (e) a diode (40) connected between the drain area and a third n+-doped region (32) in the extended gate layer. The n-doped portion constitutes a drift channel between drain and source areas. A device forming a **high voltage MOS** transistor as above is also claimed except that n-doped layers are substituted for the p-doped layers and vice versa.

USE - Useful in the fabrication of **semiconductor** transistor devices, especially **MOS** transistors with extended drift regions having modulated resistance in the drift region.

ADVANTAGE - Provides a lateral transistor for high frequency applications. The gate current is controlled and a normal control voltage for the channel may be used due to the extended drift region, which modulates the resistance in the drift region by the extra **semiconductor layer** a **top** the drift region. It is thereby possible to design a **MOS** transistor with a short channel length and an extended drift region with low doping concentration, whilst still obtaining very low on-resistance together with high breakdown voltage.

Dwg.3/6

49/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009999998
WPI Acc No: 1994-267709/199433
Related WPI Acc No: 1996-474372; 1996-491208; 1999-377862; 2000-209479; 2000-567939; 2000-614542
XRAM Acc No: C94-122310
XRPX Acc No: N94-210913
Insulated gate type **FET** device for LCD optical devices - incorporates drain electrode extension beyond insulation film, deposited in upper region over gate electrode
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: HAMATANI T; YAMAZAKI S
Number of Countries: 003 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6196500	A	19940715	JP 91174269	A	19910516	199433 B
US 5459090	A	19951017	US 92877421	A	19920501	199547
			US 93111740	A	19930825	
US 5592008	A	19970107	US 92877421	A	19920501	199708
			US 93111740	A	19930825	
			US 95504226	A	19950719	
KR 9513793	B1	19951116	KR 927237	A	19920429	199902
			KR 9528651	A	19950828	
KR 9513794	B1	19951116	KR 927237	A	19920429	199902
US 6017783	A	20000125	US 92877421	A	19920501	200012
			US 93111740	A	19930825	
			US 95504086	A	19950719	

Priority Applications (No Type Date): JP 91174269 A 19910516
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6196500	A		20	H01L-021/336	
US 5459090	A		30	H01L-021/265	Cont of application US 92877421
US 5592008	A		29	H01L-027/01	Cont of application US 92877421 Div ex application US 93111740 Div ex patent US 5459090
KR 9513793	B1			H01L-029/78	Div ex application KR 927237
KR 9513794	B1			H01L-029/786	
US 6017783	A			H01L-021/84	Cont of application US 92877421 Div ex application US 93111740 Div ex patent US 5459090

Abstract (Basic): JP 6196500 A
The **field effect transistor** is formed on a **semiconductor substrate** (1). A gate insulation film (6) is formed near the side of the gate electrode (8). Electrodes (7) are formed for source and drain. The drain electrode starting from drain domain goes all the way up to the insulation **film top** surface, formed above the gate electrode. The gate insulation film separates gate electrode from the source, drain and channel domains. Above the gate electrode, an insulation film (11) is formed. An anodised film (10) forms the side wall structure for this gate electrode.
USE/ADVANTAGE - For use in image sensors. Prevents fall in

frequency characteristics of the device and increases ON-state resistance of **FET**. Reduces boundary face level density and cell area. Increases rate of opening of LCD panel. Reduces the number of masks needed for manufacture of LCD panel. and simplifies production process.

Dwg.1/12

Abstract (Equivalent): US 5592008 A

A complementary thin film transistor pair comprising: a p-channel thin film transistor and an n-channel thin film transistor formed on an insulating surface of a **substrate**, (a) the p-channel thin film transistor comprising a first **semiconductor** layer formed on the surface and having source, drain and channel regions in it; a first gate insulating layer formed on the first **semiconductor** layer; and a first gate electrode formed on the gate insulating layer, (b) the n-channel thin film transistor comprising a second **semiconductor** layer formed on the surface and having source, drain and channel regions in it; a **second gate** insulating layer formed on the second **semiconductor** layer; and a **second gate** electrode formed on the **second gate** insulating layer, where at least side surfaces of the gate electrodes are formed with an anodic **oxide layer** of the **gate** electrodes, and the source and drain regions are offset from the corresp. gate electrode in each of the transistors.

Dwg.0/14

US 5459090 A

Complementary transistor pair comprising p-channel thin film transistor and n-channel thin film transistor is mfd. by a method in which a pair of **semiconductor** islands on an insulating surface of a **substrate** and gate electrodes (8) are formed on gate insulating layer on the **semiconductor** islands. Side surfaces of the electrodes are anodically oxidised (10) and impurity regions of a first conductivity type are formed in the islands, using gate electrodes as mask. One island and electrode is masked for second impurity of second conductivity type to be used to form a pair of impurity regions in the other island channel regions are formed between impurity regions in each island and each boundary between channel region and impurity regions is aligned with outer edge of **oxide layer**.

ADVANTAGE - Decreases number of masks required.

Dwg.1/14

49/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009245618
WPI Acc No: 1992-373036/199245
Related WPI Acc No: 1996-087162
XRAM Acc No: C92-165641
XRPX Acc No: N92-284444
Prodn. of complementary **MOS** transistor pair - involves forming layer of lightly doped **semiconductor** on **substrate**, slowly diffusing dopant into layer and rapidly diffusing dopant into layer, etc.
Patent Assignee: SILICONIX (SILI-N)
Inventor: BLANCHARD R A; WILLIAMS R K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5156989	A	19921020	US 88268839	A	19881108	199245	B

Priority Applications (No Type Date): US 88268839 A 19881108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5156989	A		45	H01L-021/265	

Abstract (Basic): US 5156989 A
Producing a complementary **MOS** transistor pair comprises: (a) providing a lightly doped **semiconductor substrate** of a first electrical conductivity type; (b) providing a covering layer of lightly doped **semiconductor** material of first conductivity type; (c) providing a slowly diffusing dopant of a second electrical conductivity type opposite to that of the first conductivity type; (d) providing a rapidly diffusing dopant of second conductivity type of a second portion of the **substrate**-covering layer interface; (e) providing a rapidly diffusing dopant of second conductivity type at a first portion of the top surface of the covering layer; (f) providing a rapidly diffusing dopant of second conductivity type at a second portion of the top surface of the covering layer that is spaced apart from and not laterally surrounded by the first portion of the top surface of the covering layer; providing two deep fifth dopant profiles of heavily doped first conductivity type extending downward from the top surface of the covering layer and not within the enclosed region; (h) providing 3 field **oxide** regions at the **top** surface of the covering layer; (i) providing a thin **oxide layer** 0.02-0.25 microns thick, over the upper surface of the structure; (j) providing three gate regions of doped **semiconductor** material on the first **oxide layer**; (k) providing a thin sixth dopant profile of lightly doped second conductivity type in the covering **layer** adjacent to its **top** surface at all portions that do not overlie the field **oxide** or **gate** regions; (l) providing **two** seventh dopant profiles of lightly doped first conductivity type in the covering **layer** adjacent to the **top** surface; (m) providing an eighth dopant profile of lightly doped second conductivity type within the enclosed region and adjacent to the top surface; (n) providing four ninth dopant profiles of heavily doped first conductivity type lying in the covering layer or the enclosed region adjacent to the top surface of the covering layer; (o) providing four

tenth dopant profiles of heavily doped second conductivity type within the covering layer or the enclosed region and adjacent to the top surface of the covering layer; and (p) providing a thick **oxide layer** over the upper surface of the structure. Pref. the structure is completed by the formation of electrodes and electrical contacts to the dopant profiles and gate regions, respectively.

USE/ADVANTAGE - Fabrication of various isolated, **high voltage** IC devices by simplified procedures which provide self isolated regions with permitted voltage differentials up to 600V, increased packing density, suppression of parasitic effects. The initial steps of the process are identical for all devices.

(Dwg.0/14

49/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008315309
WPI Acc No: 1990-202310/199027
XRAM Acc No: C90-087513
XRPX Acc No: N90-157461
Isolation of **MOS**-transistors in silicon **semiconductor substrates** - uses field-plates instead of locos grown field-oxide to red. space required and allow miniaturisation of transistors
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: EIMORI T; OZAKI H; SATOH S; TANAKA Y; WAKAMIYA W
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3942648	A	19900628	DE 3942648	A	19891221	199027	B
JP 2172253	A	19900703	JP 88327069	A	19881224	199032	
US 5164803	A	19921117	US 89450769	A	19891204	199249	
			US 91657261	A	19910219		

Priority Applications (No Type Date): JP 88327066 A 19881224; JP 88327069 A 19881224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5164803	A		12	H01L-029/06	Cont of application US 89450769

Abstract (Basic): DE 3942648 A

On the surface of a Si-**substrate** (1) a **MOS**-transistor is formed consisting of the elements **gate-oxide** (4), **gate** electrode (5), source and drain diffused regions (6). The transistor is isolated from its neighbours by a field-plate (9) on **top** of a **gate-oxide** (8), pref. thicker than the transistor **gate-oxide**, which is sepd. from the diffused regions by an **oxide spacer** (12).

The **oxide spacer** is thick enough to ensure that the parasitic **MOS**-transistor formed by the presence of the field-plate (9) has a gate offset. The field-plate electrode is biased. An implanted layer (14) is pref. present to define the threshold voltages of both parasitic and active transistors. A **CMOS** device can be built by combining n- and p-channel **MOS** transistors on the same **substrate**.

USE/ADVANTAGE - The isolation regions require less space than LOCOS isolations. They are also smaller than current field-plate isolation structures because they do not need a channel stopper under the isolation oxide. This leaves more space for the transistors, which as a result no longer suffer from the threshold voltage increase due to the narrow channel effect.

Dwg.1/7

Abstract (Equivalent): US 5164803 A

A **CMOS** device with two **MOSFET**'s has a **semiconductor substrate** with a field shield formed on an isolating region. A bias voltage applied to the shield prevents the formation of a surface inversion layer. A switching electrode in each **MOSFET** operates through a second insulating film. Source and drain regions on each side of a channel underly the switching gate

electrode. The source and drain layers are spaced and positioned so that they do not overlap the field shield. The first gate insulating film being thicker than that on the **second gate**. ADVANTAGE - The device can be miniaturised without problems due to parasitic **MOS** effects.
(Dwg.2/7

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     (FILE 'HOME' ENTERED AT 14:39:21 ON 10 DEC 2002)

     FILE 'REGISTRY' ENTERED AT 14:40:59 ON 10 DEC 2002
                E SILICON/CN
L1             1 SEA ABB=ON  PLU=ON  SILICON/CN

     FILE 'HCAPLUS' ENTERED AT 14:41:47 ON 10 DEC 2002
L2        677499 SEA ABB=ON  PLU=ON  L1 OR SI
L3        426968 SEA ABB=ON  PLU=ON  SEMICONDUCT#######
L4        117993 SEA ABB=ON  PLU=ON  L2 AND L3
L5         13778 SEA ABB=ON  PLU=ON  L4 AND (MOS OR METAL(W)OXIDE(1W)SEMICONDUCT
                  ? OR NMOS OR N(W)MOS OR PMOS OR P(W)MOS OR VMOS OR V(W)MOS OR
                  C(W)MOS OR CMOS OR NMOSFET OR NMOS(W)FET)
L6          2567 SEA ABB=ON  PLU=ON  L5 AND (DMOS(W)FET OR DMOSFET OR UMOS(W)FET
                   OR UMOSFET OR MOS(W)FET OR MOSFET)
L7          1797 SEA ABB=ON  PLU=ON  L6 AND ((FIELD(W)EFFECT(1W)TRANSIST#######)
                   OR FET)
L8             5 SEA ABB=ON  PLU=ON  L7 AND (HIGH###(W)(VOLT# OR POWER#))
L9          1796 DUP REM L7 (1 DUPLICATE REMOVED)
L10            5 DUP REM L8 (0 DUPLICATES REMOVED)
                  D BIB AB TOT
L11         1792 SEA ABB=ON  PLU=ON  L7 NOT L8
L12           60 SEA ABB=ON  PLU=ON  L11 AND ((DUAL OR TWO OR DOUBLE OR
                  SECOND)(3A)(GATE OR OPENING))
L13            0 SEA ABB=ON  PLU=ON  L12 AND (OXIDE#(3A)(VOLT# OR POWER#))
L14           21 SEA ABB=ON  PLU=ON  L12 AND SUBSTRATE
L15            9 SEA ABB=ON  PLU=ON  L14 AND (OXIDE#(3A)(LAYER### OR FILM### OR
                  COAT### OR MULTILAYER### OR SPACER###))
L16            9 DUP REM L15 (0 DUPLICATES REMOVED)
                  D BIB AB TOT
L17           12 SEA ABB=ON  PLU=ON  L14 NOT L15
L18            0 SEA ABB=ON  PLU=ON  L17 AND (BURIED(3A)OXIDE?)
L19            0 SEA ABB=ON  PLU=ON  L17 AND (TOP(3A)(LAYER### OR FILM### OR
                  COAT### OR MULTILAYER### OR SPACER###))
L20            0 SEA ABB=ON  PLU=ON  L17 AND TOP(3A)OXIDE?
L21            1 SEA ABB=ON  PLU=ON  L17 AND GATE##(3A)OXIDE?
                  D BIB AB TOT
L22           11 SEA ABB=ON  PLU=ON  L17 NOT L21
L23           11 DUP REM L22 (0 DUPLICATES REMOVED)
                  D BIB AB TOT
L24           39 SEA ABB=ON  PLU=ON  L12 NOT L14
L25            7 SEA ABB=ON  PLU=ON  L24 AND ((SILICON OR SI)(3A)(LAYER### OR
                  FILM### OR COAT### OR MULTILAYER### OR SPACER###))
L26            7 DUP REM L25 (0 DUPLICATES REMOVED)
                  D BIB AB TOT
L27           32 SEA ABB=ON  PLU=ON  L24 NOT L25
L28            7 SEA ABB=ON  PLU=ON  L27 AND SOI
L29            7 DUP REM L28 (0 DUPLICATES REMOVED)
L30            7 SEA L29
                  D BIB AB TOT
L31           25 SEA ABB=ON  PLU=ON  L27 NOT L30
L32            2 SEA ABB=ON  PLU=ON  L31 AND (SOURCE#(3A)(REGION### OR AREA))
                  D BIB AB TOT
L33           23 SEA ABB=ON  PLU=ON  L31 NOT L32
L34            0 SEA ABB=ON  PLU=ON  L33 AND (BODY(3A)(REGION### OR AREA))
L35            1 SEA ABB=ON  PLU=ON  L33 AND (DRIFT(3A)(REGION### OR AREA))
                  D BIB AB TOT
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L10 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:307035 HCAPLUS
DN 129:35305
TI SiC **semiconductor** device
IN Kataoka, Mitsuhiro; Suzuki, Takaaki
PA Nippondenso Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10125904	A2	19980515	JP 1996-275128	19961017

AB The invention relates to a **semiconductor** device, esp., a trench gate-type SiC vertical **high-power MOSFET** (**metal oxide semiconductor field effect transistor**), wherein the layout reduces ON resistance.

L10 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:328243 HCAPLUS
DN 124:358258
TI **Semiconductor** device and manufacture thereof
IN Nagata, Kenichi
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08078675	A2	19960322	JP 1994-207169	19940831
	JP 3169776	B2	20010528		

AB A **semiconductor** device, esp., a vertical **MOS FET**, suited for use in a high-speed **high-power** switching device, wherein the poly-**Si** gate contact layer contains an array of cross patterns, which increases the channel width per unit area.

L10 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:467551 HCAPLUS
DN 123:23155
TI Numerical prediction for 2 GHz RF amplifier of SOI power **MOSFET**
AU Omura, Ichiro; Nakagawa, Akio
CS Res. and Development Cent., Toshiba Corp., Kawasaki, 210, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1995), 34(2B), 827-30
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB RF performance of a **metal-oxide-semiconductor field effect transistor** (**MOSFET**) on silicon-on-insulator (SOI) with 0.5 .mu.m gate length and 2 .mu.m buried oxide thickness has been numerically predicted using a 2-D device simulator to check its applicability to digital cellular telephones. The device has been found to have excellent performance for a 2 GHz **high-power** amplifier at a power supply of 2.8 V. The calcd. cutoff frequency and max. frequency of oscillation for the intrinsic **MOSFET** are 23 GHz and GHz, resp. The SOI **MOSFET** is a promising candidate for replacing GaAs **MOSFET** 's in 2 GHz RF applications.

L10 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:546169 HCAPLUS
DN 121:146169
TI application technique of photoemission microscopy on **si** and GaAs devices
AU Tamura, T.; Noda, H.; Ooura, A.; Kanno, T.; Nakamura, M.; Matsuda, S.; Kurosaki, K.
CS Natl. Space Dev. Agency Japan, Ibaraki, Japan
SO ISTFA '93, Proc. Int. Symp. Test Failure Anal., 19th (1993), 315-19
CODEN: 59UTAD
DT Conference
LA English
AB Photoemission Microscopy has been recognized as a powerful tool to locate defects in **semiconductor** devices. In this work, the technique was applied to some **semiconductor** devices such as 1 Mbit SRAM and laser diodes(LDs) which are planned to be developed for space applications. To evaluate radiation resistance of the 1 Mbit SRAM, several Test Element Group (TEG) representing typical structure of the memory chip was fabricated and irradiated with gamma-ray. Increase of leakage current was obsd. for **n-MOS FET** TEG and the image of photoemission correlated well with the results. For 1 Mbit SRAM chip, some **n-MOS FETs** in the peripheral region were obsd. to emit photons after irradn. This also confirmed the results of TEG data. Further, to investigate the applicability of photoemission technique to another type of **semiconductor** devices, a **high power** LD was obsd. to characterize spontaneous emission below lasing threshold current. By applying photon counting method, a sign of degrdn. which could not be detected by another method was detected. By this technique, it may be possible to find LDs with higher potential to degrade faster than usual.

L10 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1976:601120 HCAPLUS
DN 85:201120
TI A **high power MOS-FET** with a vertical drain electrode and meshed gate structure
AU Yoshida, Isao; Kubo, Masaharu; Ochi, Shikayuki; Ohmura, Yoshito
CS Cent. Res. Lab., Hitachi Ltd., Tokyo, Japan
SO Proc. Conf. Solid State Devices (1975), 7, 179-83
CODEN: PCSDDB
DT Journal
LA English
AB The p-channel **metal-oxide-semiconductor field-effect-transistor** (**MOS FET**) device with an offset gate structure was fabricated from an n-on-p+ epitaxial **Si** wafer by using the polycryst. **Si** gate and the ion implantation processes. The device does not show local current crowding, thermal runaway, or 2nd breakdown. Stable operation is obtained at ambient temps. as high as 180.degree., which is attributed to a neg. temp. coeff. of the drain current. The vertical drain electrode allows most of the surface area to be used for the source electrode. The meshed gate makes it possible for the channel width per unit area to be twice as large as in conventional **MOS FETs**, thereby increasing the drain current.

L30 ANSWER 6 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:265206 HCAPLUS
DN 130:274860
TI Scaling parameter dependent drain induced barrier lowering effect in **double-gate** silicon-on-insulator **metal-oxide-semiconductor field effect transistor**
AU Samudra, Ganesh; Rajendran, Krishnasamy
CS Department of Electrical Engineering, Faculty of Engineering, National University of Singapore, Singapore, 119 260, Singapore
SO Japanese Journal of Applied Physics, Part 2: Letters (1999), 38(4A), L349-L352
CODEN: JAPLD8; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A simple model equation to study the effect of drain induced barrier lowering (DIBL) parameters on device performance for a **double-gate** silicon-on-insulator (**SOI**) **metal-oxide-semiconductor field effect transistor** (**MOSFET**) is proposed. This model equation is used to study the influence of various device parameters on the DIBL effect. The main conclusions drawn from the present study are that (a) two different approaches for detg. the DIBL parameter lead to the same model equation and (b) it is easier to calc. the DIBL parameter rather than ext. it from the current-voltage plots. This model is also easy to implement in a circuit simulator. It is found that the DIBL parameter is almost inversely proportional to the channel length and directly proportional to the gate oxide and silicon thickness. It is shown that a DIBL parameter of less than 0.1 down to a gate length of 0.1 .mu.m is possible at lower **Si** thicknesses.
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 5 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:150789 HCAPLUS
DN 134:274078
TI Investigation of deep submicron single and **double gate** **SOI MOSFETs** in accumulation mode for enhanced performance
AU Rauly, E.; Iniguez, B.; Flandre, D.
CS Microelectronics Laboratory, Universite Catholique de Louvain, Louvain la Neuve, B1348, Belg.
SO Electrochemical and Solid-State Letters (2001), 4(3), G28-G30
CODEN: ESLEF6; ISSN: 1099-0062
PB Electrochemical Society
DT Journal
LA English
AB The behavior of single and **double gate** accumulation mode silicon-on-insulator (**SOI**) **metal oxide semiconductor field effect transistors** (**MOSFETs**) is thoroughly investigated. Accumulation mode devices present advantages over inversion mode transistors regarding transconductance, ease of fabrication, and parasitic effects. We have concluded, from exptl. results and 2D simulations, that short channel effects such as DIBL and subthreshold swing degrdn. are substantially reduced in the vol. accumulation regime, being even lower in thin-film **double gate** accumulation mode **SOI** **MOSFETs** than in inversion mode **double gate** **SOI** devices for adequate technol. characteristics. The potential of thin-film accumulation mode **SOI MOS** transistors down to sub-0.1 .mu.m technologies and up to 125.degree.C is demonstrated.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L26 ANSWER 3 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:999646 HCAPLUS
DN 124:43286
TI **Semiconductor** device and manufacture thereof
IN Warashina, Taku
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 07263701	A2	19951013	JP 1994-48115	19940318

AB A **semiconductor** device, esp., a double-gated **MOS FET**, wherein the source-drain region is formed in the active **Si layer** in the SOI chip, to reduce the overlap capacitance created between the gate and the source-drain.

L26 ANSWER 4 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:179437 HCAPLUS
DN 120:179437
TI Coulomb blockade in the inversion **layer** of a **Si metal-oxide-semiconductor field-effect transistor** with a **dual-gate** structure
AU Matsuoka, Hideyuki; Ichiguchi, Tsuneo; Yoshimura, Toshiyuki; Takeda, Eiji
CS Cent. Res. Lab., Hitachi Ltd., Kokubunji, 185, Japan
SO Applied Physics Letters (1994), 64(5), 586-8
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB The transport properties were studied of artificially squeezable inversion **layers** in a **Si MOS FET** with a **dual-gate** structure. Increasing the potential barrier height with const. intervals along the 1-dimensional channel gradually transforms a simple quantum wire into coupled quantum dots. The change in transport properties was obsd. by changing the tunnel barrier height at low temps. The exptl. results are discussed in terms of 1-dimensional subbands and the Coulomb blockade of single-electron tunneling.

L16 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:290741 HCAPLUS
DN 136:302771
TI Simple method for fabricating self-aligned vertical **double-gate MOSFET**
IN Crowder, Scott; Hargrove, Michael J.; Ku, Suk Hoon; Logan, L. Ronald
PA International Business Machines Corporation, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6372559	B1	20020416	US 2000-709073	20001109

AB A method of forming a self-aligned vertical **double-gate metal oxide semiconductor field effect transistor** (**MOSFET**) device is provided that includes processing steps that are **CMOS** compatible. The method include the steps of growing an **oxide layer** on a surface of a **Si**-on-insulator (SOI) **substrate**, said SOI **substrate** having a buried oxide region located between a top **Si**-contg. layer and a bottom **Si**-contg. layer, wherein said top and bottom **Si**-contg. layers are of the same cond.-type; patterning and etching gate openings in said **oxide layer** , said top **Si**-contg. **layer** and said buried **oxide** region stopping on said bottom **Si**-contg. layer of said SOI **substrate**; forming a gate dielec. on exposed vertical sidewalls of said gate openings and filling said gate openings with **Si**; removing oxide on horizontal surfaces which interface with said **Si**-contg. bottom layer; recrystg. **Si** interfaced to said gate dielec. and filling said gate openings with epitaxial **Si**. Forming a mask on said **oxide layer** so as cover one of the **Si** filled gate openings, while leaving an adjacent **Si** filled gate opening exposed; selectively implanting dopants of said 1st cond.-type into said exposed **Si** filled gate opening and activating the same, wherein said dopants are implanted at an ion dosage of .apprx.1015 cm-2 or greater; selectively etching the exposed **oxide layer** and the underlying top **Si**-contg. layer of said SOI **substrate** stopping on said buried **oxide layer**; removing said mask and implanting a graded-channel dopant profile in said previously covered **Si** filled gate opening; etching any remaining **oxide layer** and forming **spacers** about said **Si** filled gate openings; and saliciding any exposed **Si** surfaces.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:466480 HCAPLUS
DN 137:27020
TI **CMOS** DRAM **MOSFET** VLSI and fabrication thereof
IN Furuta, Haruo; Yamashita, Tomohiro
PA Mitsubishi Denki Kabushiki Kaisha, Japan
SO U.S. Pat. Appl. Publ., 29 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002074614	A1	20020620	US 2001-14345	20011214
	JP 2002246481	A2	20020830	JP 2001-359269	20011126
PRAI	JP 2000-381822	A	20001215		

AB A **semiconductor** device and a method of manufg. the **semiconductor** device, which **semiconductor** device comprises grooves formed on a main surface of a **semiconductor substrate**, silicon **oxide films** embedded in insides of the grooves, a first active region surrounded by the grooves and disposed on a first portion of the main surface of the **semiconductor substrate**, a first **field effect transistor** having a first gate **oxide film** formed on a main surface of the first active region, a second active region surrounded by the grooves and disposed on a second part on the main surface of the **semiconductor substrate**, and a second **field effect transistor** having a **second gate oxide film**, having a thickness different from that of the first gate **oxide film**, formed on a main surface of the second active region, wherein end shapes of the first active region and second active region are the same, by which drops of the silicon **oxide films** in the grooves along edges of the grooves do not occur.

L16 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:917912 HCAPLUS
DN 136:30374
TI Method for manufacturing **MOS field effect transistors**
IN Yun, Kyung Il; Heo, Yong Jin
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000004367	A	20000125	KR 1998-25799	19980630

AB A fabrication method of an **MOS field effect transistor** having a lightly doped drain structure is provided to prevent downing of threshold voltage and remove trade-off between punch-through voltage and cond. by using **double gate** polysilicon and a native oxide. The method comprises the following steps: forming a gate oxide on a **Si substrate**; forming a 1st polysilicon **layer** on the gate **oxide**; growing a native oxide on the 1st polysilicon layer; forming a 2nd polysilicon layer having thick thickness compared to the 1st polysilicon **layer** on the native **oxide**; exposing a portion of the 1st polysilicon layer; forming a lightly doped impurity region by ion-implantation into the exposed polysilicon layer; forming a spacer at both sides of the native **oxide** and the polysilicon **layers**; exposing a portion of the lightly doped impurity region by blanket etching the exposed 1st polysilicon; forming an SELOCS (SELective **Oxide Coating** of **Si**-gate) **oxide** at sides of the 1st polysilicon layer; and forming highly doped impurity regions.

L16 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:256368 HCAPLUS
DN 124:330010
TI **Semiconductor** device and its manufacture
IN Yamada, Kenji
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08046063	A2	19960216	JP 1994-174945	19940727

AB In the device comprising (A) a **semiconductor substrate** ; (B) first insulating film (formed at the first region on the **substrate**) successively laminated with floating **gate** first conductive film, **second** insulating film, and control **gate second** conductive film; and (C) third insulating film (formed at the second region on the **substrate**, as neighbor of the first region) laminated with a gate third conductive film; the third conductive film is formed by same process forming the first- and second conductive film, and they are elec. connected. In the manuf. of the device, the first- and third conductive films are first formed by the same step, and lately, formed multilayered laminate of the insulating films and conductive films are etched to separatedly form the first- and second electrodes. In the manuf. of the device comprising a nonvolatile memory device at the first region, and a **FET** at the second region, the third conductive film comprises two layers from the first conductive film and the second conductive film. The method is applied to manuf. of EPROM or E2PROM with **MOSFET**.

L16 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:81692 HCAPLUS
DN 124:162435
TI Self-aligned **double-gate MOS FET** transistors and fabrication thereof
IN Horiuchi, Katsutada
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07321324	A2	19951208	JP 1994-105307	19940519

AB The fabrication involves forming a single-cryst.-**semiconductor/oxide/semiconductor/oxide/substrate multilayer** SOI **substrate**, patterning a single-cryst.-**semiconductor/oxide/semiconductor layers** over an upper gate electrode as a mask, and forming a buried gate electrode by doping from the **semiconductor** film. The process provides the **MOS** transistors with decreased parasitic resistance.

L16 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:605445 HCAPLUS
DN 122:328437
TI Manufacture of **CMOS** devices with metal silicide gate electrodes
IN Kato, Juri; Tanaka, Kazuo
PA Seiko Epson Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 17 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06310667	A2	19941104	JP 1993-180852	19930624
	JP 2002093923	A2	20020329	JP 2001-221953	19930624
	JP 2002246482	A2	20020830	JP 2001-383516	19930624
	US 5879979	A	19990309	US 1995-412939	19950329
	US 5641983	A	19970624	US 1995-548380	19951026
	US 6156592	A	20001205	US 1998-141026	19980827
PRAI	JP 1992-205203	A	19920731		
	JP 1992-205204	A	19920731		
	JP 1993-33645	A	19930223		
	JP 1993-180852	A3	19930624		
	US 1993-99592	B3	19930730		
	US 1995-412939	A1	19950329		

AB In manuf. of title **CMOS** device comprising a **Si substrate**, a n-channel **MOS** device having n-type source/drain regions and a gate **oxide film** with a gate electrode on the **Si substrate**, a p-channel **MOS** device having p-type source/drain regions and a gate **oxide film** with a gate electrode on the **Si substrate**, and a gate wiring layer elec. connecting the **gate** electrodes of the **two MOS** devices, a metal silicide layer is formed in either the gate electrode and/or the wiring layer, and no region in the gate electrodes and the gate wiring layer is doped with > 3 X 1020 cm-3 III or V impurity. Highly reliable **CMOS** devices are manufd. Manuf. processes are claimed.

L16 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:358698 HCAPLUS
DN 122:120822
TI **Semiconductor** devices with **double-gate** SOI **MOS FETs**
IN Ando, Naryoshi
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06181312	A2	19940628	JP 1992-334411	19921215

AB The process involves forming a back-gate electrode on a **substrate** over thermal and deposited **oxide films**, forming a p-SOI layer over the back-gate **oxide films**, and prepg. a front-gate electrode. Connecting electrodes are formed in contact holes. The gates and connecting electrodes are made of refractory metals or doped polycrystal **Si**.

L16 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:522829 HCAPLUS
DN 117:122829
TI Manufacture of double diffusion-type **MOS FET**
IN Takechi, Eiji
PA Oki Denki Kogyo K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04065132	A2	19920302	JP 1990-176344	19900705

AB The manuf. comprises the steps of: (1) selectively forming a 2nd cond.-type 1st diffusion layer on a 1st cond.-type **semiconductor substrate**; (2) forming a gate **oxide film** and a 1st cond.-type polycryst. **Si** film on the **substrate**; (3) selectively removing the gate **oxide film** and the polycryst. **Si** film (which will be gate electrodes) to form openings over the 1st diffusion layers; (4) implanting a 2nd cond.-type impurity through said openings to form a 2nd diffusion layers; (5) obliquely implanting a 1st cond.-type impurity to form a 3rd diffusion layers; and (6) forming a metal interconnection, connecting the 1st and 3rd diffusion layers but insulated from the gate electrodes.

L16 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:258066 HCAPLUS
DN 114:258066
TI Conductivity-modulating horizontal **MOS field-effect transistors**
IN Seki, Yasukazu
PA Fuji Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 02267969	A2	19901101	JP 1989-89050	19890407

AB The title insulated gate bipolar **MOS** transistor has (1) a low doped and lifetime-shortened 1st cond.-type **semiconductor substrate** having selectively formed 2nd cond.-type well and 1st cond.-type buffer layer set apart on its surface, (2) a highly doped 2nd cond.-type contact region and a 1st cond.-type source region which are formed on the well region and short-circuited each other on their surface by a source contact, (3) a gate contact via a gate **oxide film** formed on a surface area between the source and **substrate** regions across the well region, and (4) a highly doped 2nd cond.-type drain selectively formed on the buffer region and laminated with a drain contact, wherein a 2nd gate contact is provided via a gate **oxide film** on an exposed **substrate** surface between the well and the buffer regions to form a low-resistant flip-over region. The flip-over region in the transistor gives a steep current increased in a low voltage without decreasing switching speed.

L21 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:565523 HCAPLUS
DN 125:262371
TI Ultrastable emission from a **metal-oxide-semiconductor field-effect transistor** -structured **Si** emitter tip
AU Itoh, Junji; Hirano, Takayuki; Kanemaru, Seigo
CS Electrotechnical Laboratory, Tsukuba, 305, Japan
SO Applied Physics Letters (1996), 69(11), 1577-1578
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB A silicon field emitter tip with a **dual-gate metal-oxide-semiconductor field-effect transistor** (**MOSFET**) structure was fabricated and demonstrated. The present tip structure is just the same as an n-channel **MOSFET** whose drain was replaced by a cone-shaped **Si** tip. **Two** coplanar **gates** of 0.3-.mu.m-thick Nb are made on a 0.6-.mu.m-thick thermally oxidized SiO2 insulator between the source and the tip and make inversion layers in a p-type **Si substrate** under each gate. One of the gates has a 1.8-.mu.m-diam. aperture surrounding the tip for extn. of electrons from the tip. The other is 3 .mu.m wide and 300 .mu.m long and is sepd. by 2 .mu.m from this gate. Ultrastable emission of about 0.3 .mu.A was demonstrated with a single tip for one day.

L23 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:770101 HCAPLUS
DN 137:287504
TI Power **MOS** device with improved gate charge performance
IN Calafut, Daniel S.
PA Fairchild Semiconductor Corporation, USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6461918	B1	20021008	US 1999-468269	19991220

AB A double-diffused **metal-oxide-semiconductor** (DMOS) **field-effect transistor** with an improved gate structure. The gate structure includes a 1st portion of a 1st cond. type for creating electron flow from the source to the drain when a charge is applied to the gate. The gate structure includes a 2nd portion of a 2nd cond. type having a polarity that is opposite a polarity of the 1st cond. type, for decreasing a capacitance charge under the gate. A 2nd structure for decreasing a capacitance under the gate includes an implant region in the **semiconductor substrate** between a channel region, where the implant region is doped to have a cond. opposite the channel region.

RE.CNT 32 THERE ARE 32 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:237322 HCAPLUS
DN 136:255801
TI Dual amorphization process optimized to reduce gate line over-melting during annealing in fabrication of integrated circuits
IN Yu, Bin
PA Advanced Micro Devices, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6361874	B1	20020326	US 2000-597623	20000620

AB A method of fabricating an integrated circuit with ultra-shallow source/drain junctions uses a dual amorphization technique. The technique creates a shallow amorphous region and a deep amorphous region 300 nm thick. The shallow amorphous region can be between 10-15 nm below the top surface of the **substrate**, and the deep amorphous region can be between 150-200 nm below the top surface of the **substrate**. The process can reduce gate over-melting effects. The process can be used for P-channel or N-channel **metal oxide semiconductor field effect transistors** (**MOSFETs**).
RE.CNT 43 THERE ARE 43 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:105115 HCAPLUS
DN 136:159875
TI Manufacture of **dual-gate CMOS-FETs**
IN Kubo, Hiroko; Yoneda, Kenji
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 18 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002043566	A2	20020208	JP 2000-226559	20000727
	US 2002019101	A1	20020214	US 2001-911618	20010725
PRAI	JP 2000-226559	A	20000727		

AB The process includes: (a) forming SiGe layers on **semiconductor substrates** across gate insulator films, (b) forming amorphous **Si** layers on the SiGe layers, and (c) patterning the laminated SiGe/**Si** layers into gate electrodes. Impurities implanted in the gate electrodes are prevented from infiltration into the **substrates**.

L23 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:560101 HCAPLUS
DN 135:115637
TI DMOS **field effect transistor** with improved electrical characteristics and method for manufacturing the same
IN Jeon, Chang Ki
PA Fairchild Korea Semiconductor Ltd., S. Korea
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6268626	B1	20010731	US 2000-478800	20000107
	KR 2000051294	A	20000816	KR 1999-1648	19990120
PRAI	KR 1999-1648	A	19990120		

AB In a double diffused **MOS (DMOS) FET** according to the present invention, a drift region of a 1st cond. type is formed on a **semiconductor substrate**. A gate electrode is formed over the drift region, interposing a gate insulating layer between the drift region and the gate electrode. The gate electrode includes a gate conductive layer and a conductive spacer formed on the side wall of the gate conductive layer. A body region is formed to be self-aligned by the gate conductive layer. The source region is formed to be self-aligned by the conductive spacer. A doping profile in a channel region of the body region has a form in which a uniform doping d. value is maintained. Although the threshold voltage of the device is lowered by reducing the peak doping d., the d. of impurities in the channel region is not decreased. A punch-through characteristic is not deteriorated.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:457325 HCAPLUS
DN 133:67311
TI Metal **gate double**-diffused **MOSFET** with improved switching speed and reduced gate tunnel leakage
IN Chau, Duc Q.; Mo, Brian S.
PA Fairchild Semiconductor Corporation, USA
SO PCT Int. Appl., 22 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000039858	A2	20000706	WO 1999-US29423	19991210
	WO 2000039858	A3	20001221		
	W: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	US 2002084486	A1	20020704	US 2002-53891	20020111
PRAI	US 1998-222258	A	19981228		

AB A double-diffused **metal-oxide-semiconductor** (DMOS) **field-effect transistor** with a metal gate. A sacrificial gate layer is patterned to provide a self-aligned source mask. The source regions are thus aligned to the gate, and the source diffusion provides a slight overlap for good turn-on characteristics and low leakage. The sacrificial gate layer is capable of withstanding the diffusion temps. of the DMOS process and is selectively etchable. After the high-temp. processing is completed, the sacrificial gate layer is stripped and a metal gate layer is formed over the **substrate**, filling the vol. left by the stripped sacrificial gate material. In one embodiment, a chem.-mech. polishing technique is used to planarize the metal gate layer.

L23 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:91999 HCAPLUS
DN 124:162430
TI SOI **substrate** and fabrication thereof
IN Hashimoto, Makoto
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07321297	A2	19951208	JP 1994-131250	19940521

AB A SOI **substrate**, suited for use in fabrication of **semiconductor** devices, esp., a double-gated **MOS FET**, wherein the strains introduced during the processing are eliminated for optimum performance.

L23 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:418846 HCAPLUS
DN 119:18846
TI Manufacture of integrated circuits containing **MOS field -effect transistors** with **double**-layer **gate** electrodes
IN Tanaka, Kota; Shiba, Kazuyoshi; Kuroda, Kenichi; Hashimoto, Koichiro
PA Hitachi, Ltd., Japan; Hitachi Device Engineering K. K.; Hitachi Maikon System K. K.
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04352367	A2	19921207	JP 1991-124308	19910529
JP 3067838	B2	20000724		

AB In the process, an elec. conductive film (e.g., poly-**Si**) for floating gates formed on a **semiconductor substrate** and patterned in a lattice configuration, an insulator film, and a 2nd elec. conductive film (e.g., poly-**Si**) for control gates are successively formed and the laminate is etched to create double-layer floating and control gates.

L23 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:203443 HCAPLUS
DN 118:203443
TI Manufacture of **dual-gate MOS field -effect transistors**
IN Sukegawa, Kazuo; Ishigaki, Toru
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04290473	A2	19921015	JP 1991-54829	19910319

AB The process includes the steps of: (a) forming a 1st gate-insulator film on a **semiconductor substrate**; (b) forming a 1st gate-electrode layer on the insulator film; (c) forming a light-shielding film on the gate-electrode layer; (d) patterning the light-shielding film, the gate-electrode layer, and the gate-insulator film to create a 1st gate part on the **substrate**; (e) forming an insulator film on the **substrate** the 1st gate to planarize the whole surface; (f) attaching a transparent **substrate** to the planar insulator film; (g) polishing the **substrate** from its bottom side to create a device layer; (h) forming a 2nd gate-insulator film on the device layer; (i) forming a 2nd gate-electrode layer on the 2nd gate-insulator film; (j) forming a p-resist film on the 2nd gate-electrode layer; (k) applying light from the transparent-substate side for the exposure of the p-resist film with the light-shielding film on the 1st gate part; and (l) etching the 2nd gate-electrode layer and the 2nd gate-insulator film with the patterned p-resist film as a mask to create a 2nd gate part.

L23 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:643926 HCAPLUS
DN 117:243926
TI Horizontal double-diffused **MOS field-effect transistors**
IN Hoshi, Masakatsu
PA Nissan Motor Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04142078	A2	19920515	JP 1990-263165	19901002

AB A horizontal double-diffused **MOSFET** contains (a) a trench formed in a 1st-cond.-type **semiconductor substrate**; (b) a 2nd-cond.-type base region under the trench; (c) a 1st-cond.-type source region in the surface of the base region; (d) a drain region in the **substrate** surface near the trench; and (e) a gate electrode stretching from the surface of the source region to over the trench sidewall across a gate-insulator film. The **MOSFET** can be fine-scaled, and have decreased on-resistance.

L23 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:462054 HCAPLUS
DN 115:62054
TI **Metal-oxide semiconductor** transistors fabricated on silicon/aluminum oxide/silicon structures
AU Ishida, M.; Yamaguchi, S.; Masa, Y.; Nakamura, T.; Hikita, Y.
CS Dep. Electr. Electron. Eng., Toyohashi Univ., Toyohashi, 440, Japan
SO Journal of Applied Physics (1991), 69(12), 8408-10
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB **Metal-oxide semiconductor field effect transistors** (**MOSFETs**) were fabricated by using a polycryst.-**Si gate** process on **double** heteroepitaxially grown **Si**(100)/Al2O3(100)/**Si**(100) structures in order to characterize the **Si**-on-insulator (SOI) structures. To realize the SOI structures, at first, the epitaxial Al2O3(100) film was grown on a 2-in. **Si**(100) wafer, and then, **Si** epitaxial film was grown on the Al2O3/**Si** by the chem. vapor deposition method. The SOI wafers were able to be handled in the same way as **Si** wafers during the device fabrication process. From ID-VD and ID-VG properties of the **MOSFET**, the transistor action was confirmed, and the threshold voltage of 0.4 V and the effective mobility of 540 cm2/V s at VG - VT = 4.0 V were obtained. The epitaxial **Si** layer was p-type, and the impurity concn. was considered to be 5 .times. 1015 cm-3. These results were very similar to those obtained from **Si** on sapphire epitaxial films.

L23 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:14944 HCAPLUS
DN 108:14944
TI **Semiconductor** apparatus with a device having a passivation film
IN Yamazaki, Koji
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 62174927	A2	19870731	JP 1986-17115	19860128

AB A **semiconductor** device formed on a **semiconductor substrate** is coated with a 2-layer passivation film composed of a F-contg. **Si** nitride lower layer formed by plasma chem. vapor deposition (CVD) and a **Si** nitride upper layer formed from SiH4 with NH3 or N2 by plasma CVD to obtain a **semiconductor** app. The passivation film gives the app. excellent humidity resistance and stable gate threshold voltage. A F-contg. **Si** nitride lower film was formed on a **MOS FET** device from Si2F6 and N2 by plasma CVD and a **Si** nitride upper film was formed on the lower film from SiH4, NH3, and N2 by plasma CVD to obtain a **MOS FET** bearing a 2-layer passivation film for excellent humidity resistance.

L26 ANSWER 1 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:287009 HCAPLUS
DN 132:287040
TI Characteristic length of hot-electron transport in silicon **metal -oxide-semiconductor field-effect transistors**
AU Sakamoto, T.; Kawaura, H.; Baba, T.; Iizuka, T.
CS Fundamental Research Laboratories, NEC Corp., Tsukuba, Ibaraki, 305-8501, Japan
SO Applied Physics Letters (2000), 76(18), 2618-2620
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Characteristic length of hot-electron transport in an inversion **layer** at a **Si** surface is estd. by using lateral hot electron transistor, which has an upper **gate** and **two** lower **gates**. The inversion layer formed by biasing the upper-gate voltage is sepd. into three channel regions (the emitter, collector, and base) by the **two** lower **gates**. We find that the characteristic length depends on both the upper-gate voltage and the injection energy and ranges from 19 to 27 nm. These results show that hot electrons are affected by electron-electron scattering or surface-roughness scattering and that hot-electron transport plays a crucial role in **Si metal-oxide-semiconductor field effect transistors** (**MOSFETs**) with gate lengths of .ltoreq.20 nm.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L26 ANSWER 2 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:756937 HCAPLUS
DN 131:359187
TI **Semiconductor** integrated circuits having **metal-oxide-semiconductor field-effect transistors** and their manufacture
IN Tanabe, Yoshikazu; Yamamoto, Naoki; Mitani, Shinichiro; Hanaoka, Hiroko
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 20 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11330468	A2	19991130	JP 1998-138939	19980520
	SG 75953	A1	20001024	SG 1999-2151	19990507
	EP 964437	A2	19991215	EP 1999-303683	19990510
	EP 964437	A3	20021127		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	CN 1236186	A	19991124	CN 1999-106677	19990520
	US 6323115	B1	20011127	US 1999-314956	19990520
	US 2002004263	A1	20020110	US 2001-929091	20010815
PRAI	JP 1998-138939	A	19980520		
	US 1999-314956	A3	19990520		

AB The circuits are manufd. by (1) forming B-doped polycryst. **Si films** on gate-insulating **films** contg. **Si** oxide **films** of **Si** wafers, (2) forming W-based high-m.p. metal **films** on the **Si films** directly or via barrier **layers**, (3) patterning the **Si films** and the high-m.p. metal films to form gate electrodes, and (4) thermally oxidizing the **Si** wafers and the **Si films** at end parts of the gate electrodes in a mixed atm. contg. H and water vapor. The obtained devices are also claimed. In **CMOS**-type integrated circuits having polymetal **gate** structures and **dual gate** structures, oxidn. of the high-m.p. metal films and diffusion of B in the **Si films** are prevented.

L26 ANSWER 5 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:92241 HCAPLUS
DN 120:92241
TI Analytical models for symmetric thin-**film double-gate silicon**-on-insulator **metal-oxide -semiconductor field-effect transistors**
AU Suzuki, Kunihiro; Satoh, Shigeo; Tanaka, Tetsu; Ando, Satoshi
CS Fujitsu Lab., Atsugi, 243-01, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1993), 32(11A), 4916-22
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
AB The authors derived anal. models for the current-voltage characteristics of **double-gate** silicon-on-insulator MESFET transistors. In the subthreshold region, they drived an anal. subthreshold slope model considering both depleted and induced charges. They proposed a unique definition of threshold voltage of the device, and showed that the threshold voltage is close to the exptl. defined threshold voltage at which the drain current has a specific value. The variation in the surface potential after the threshold voltage was modeled, and hence the models are valid in the moderate-inversion region as well as in the strong inversion region. The models agree well with exptl. data.

L26 ANSWER 6 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:548259 HCAPLUS
DN 115:148259
TI Manufacture of **semiconductor** device having lightly doped drain structure
IN Kurosawa, Susumu
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03055849	A2	19910311	JP 1989-191737	19890724

AB Described is manuf. of a lightly doped drain **semiconductor** device (e.g., **MOS FET**), in which a **double** -layer-structure **gate** electrode consists of a high-m.p. metal-silicide film and an n+-cond.-type polycryst. **Si** **film** to give a large etching speed ratio so that the self-aligned lightly doped drain can be fabricated directly beneath the gate electrode.

L26 ANSWER 7 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:638979 HCAPLUS
DN 101:238979
TI Self-aligned field implant for oxide-isolated **CMOS FET**
IN Hu, Genda J.
PA International Business Machines Corp. , USA
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4471523	A	19840918	US 1983-490766	19830502
	JP 59204232	A2	19841119	JP 1984-5862	19840118
	JP 02044154	B4	19901002		
	EP 127335	A1	19841205	EP 1984-302894	19840430
	EP 127335	B1	19870902		
	R: DE, FR, GB				
PRAI	US 1983-490766		19830502		

AB Complementary **MOS** structures are produced by using released oxide regions and highly doped n and p regions to provide isolation. The highly doped regions are self-aligned to the edges of wells produced in a **semiconductor** wafer contg. the **CMOS** structure. An optimum integrated CMDS structure is provided with a min. no. of masking steps, wherein self-alignment, high d., and optimum doping levels are provided. The use of single-crystal **Si** and its oxides and nitrides, together with a poly-**Si** gate provides a fabrication process and product with many advantages. A process for making an integrated structure comprised of complementary **MOS** devices is described, where elec. isolation is provided by recessed field oxide regions and by field isolation implant regions. Starting with a single cond. type **semiconductor** layer, such as p-type **Si**, a first masking step is used to produce an n-type well therein. After this, a **layer** of **Si** or silicide is formed through the same mask. In a **second** masking step, **openings** are made for the field isolation implant regions. The edge of the **Si** or silicide **layer** dets. the edge of the field isolation implant, which is therefore self-aligned to the edge of the well. This same mask is later used to det. the locations of the recessed oxide isolation regions. Subsequent masking steps are used to form poly-**Si** gate electrodes, source and drain regions of the active devices, contact holes and contact metal and interconnects. A high d. structure is provided without an extra masking step, and the cond. levels of the well and the field isolation implants can be sep. established. No addnl. masking steps are required for adjusting the threshold voltages of the p and n channel devices.

L30 ANSWER 1 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:604630 HCAPLUS
DN 137:360914
TI Fabrication of single-electron tunneling transistors with an electrically formed Coulomb island in a silicon-on-insulator nanowire
AU Kim, Dae Hwan; Sung, Suk-Kang; Kim, Kyung Rok; Lee, Jong Duk; Park, Byung-Gook
CS School Engineering, Inter-University Semiconductor Res. Center, Kwanak, S. Korea
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (2002), 20(4), 1410-1418
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
AB For the purpose of controllable characteristics, **Si** single-electron tunneling transistors with an elec. formed Coulomb island are proposed and fabricated from the sidewall process technique. The fabricated devices are based on a **Si**-on-insulator (**SOI**) **metal-oxide-semiconductor** (**MOS**) **field effect transistor** with the depletion gate. The key fabrication technique consists of two sidewall process techniques. One is the patterning of a uniform **SOI** nanowire, and the other is the formation of n-doped polysilicon sidewall depletion gates. While the width of a Coulomb island is detd. by the width of a **SOI** nanowire, its length is defined by the sepn. between **two** sidewall depletion **gates** which are formed by a conventional lithog. process combined with the 2nd sidewall process. These sidewall techniques combine the conventional lithog. and process technol., and guarantee the compatibility with complementary **MOS** process technol. Also, crit. dimension depends not on the lithog. limit but on the controllability of CVD and reactive-ion etching. Very uniform weakly p-doped **SOI** nanowire defined by the sidewall technique effectively suppresses unintentional tunnel junctions formed by the fluctuation of the geometry or dopant in **SOI** nanowire, and the Coulomb island size dependence of the device characteristics confirms the good controllability. A voltage gain larger than one and the controllability of Coulomb oscillation peak position are also successfully demonstrated, which are essential conditions for the integration of a single-electron tunneling transistor circuit. Further miniaturization and optimization of the proposed device will make room temp. designable single-electron tunneling transistors possible in the foreseeable future.
RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 2 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:6359 HCAPLUS
DN 136:62581
TI Doping fabrication of dual work-function **MOSFETs** with borderless diffusion contacts for high-performance embedded DRAM technology
IN Mandelman, Jack A.; Dyer, Thomas Walter
PA International Business Machines Corp., USA
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6335248	B1	20020101	US 2001-845665	20010430

AB The present invention provides a method for forming dual work-function **metal oxide semiconductor field effect transistors** (**MOSFETs**) which uses processing steps that solve the problem of doping the dual work function **MOSFETs**, while providing contacts to the diffusion regions which are borderless to the gate conductors. Specifically, the present invention provides a method wherein a self-aligned insulating gate cap is formed on top of a previously defined and doped gate conductor region. The inventive method which forms an insulating cap that is self-aligned to an underlying gate conductor enables the formation of **dual** work-function **gate** conductors and borderless diffusion contacts without the need of employing sep. block masks as required by prior art processes.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 3 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:483358 HCAPLUS
DN 135:281095
TI Modeling of minimum surface potential and sub-threshold swing for grooved-gate **MOSFETs**
AU Rajendran, K.; Schoenmaker, W.
CS STDI/TCAD Division, IMEC vzw, Louvain, B-3001, Belg.
SO Microelectronics Journal (2001), 32(8), 631-639
CODEN: MICEB9; ISSN: 0026-2692
PB Elsevier Science Ltd.
DT Journal
LA English
AB We present a new anal. model derived from Poisson equation for the min. surface potential (.PHI.m) and sub-threshold swing (S) for grooved-gate **metal oxide semiconductor field effect transistor** (**MOSFETs**). The relationship between the groove corner radius (r0), corner angle (.alpha.) and device characteristic length (.lambda.) is given. The model can be used to find a lower value of r0 at which smaller potential barrier height can be achieved in grooved-gate **MOSFETs** compared to other planar and **double-gate** devices. The study confirms that the present device is resistant to potential barrier lowering, and is also considerably strong. Sub-threshold swing values of the present device are found to be lower than that of the **double-gate** **SOI MOSFETs**, confirming the same from device simulator.
RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 4 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:422530 HCAPLUS
DN 135:188305
TI Nitrided thermal SiO2 for use as top and bottom gate insulators in self-aligned **double gate** silicon-on-insulator **metal-oxide-semiconductor field effect transistor mosfet**
AU Ahmed, Shibly S.; Denton, John P.; Neudeck, Gerold W.
CS School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 47907, USA
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (2001), 19(3), 800-806
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
AB Nitrided thermal oxide was used to reduce the degrdn. of top and bottom gate insulators of self-aligned **double gate metal-oxide-semiconductor field effect transistors** that use a form of selective epitaxial growth of silicon (SEG) called tunnel epitaxy. **SOI**. The degrdn. of thermal oxide was due to the exposure of gate insulator to the epi-growth ambient gases during the epitaxial growth. Both thermal oxide and thermally nitrided oxide samples were exposed to the epi-reactor gases and then the elec. characteristics were measured. Nitrided oxide showed significantly higher breakdown field, lower leakage current, and lower interface states than the thermal oxide after exposure to the selective epi-growth environment. For a 30 min stress in epi-reactor ambient, thermal oxide showed av. breakdown fields of less than 1 MV/cm due to the formation of pinholes, while nitrided oxide samples showed av. breakdown fields of 15.6 MV/cm for same stress condition. Interface state d. (Dit) of nitrided oxide improved after exposure to epitaxial growth ambient. The av. Dit reduced from .apprx.3.5.times.1010/cm2 eV to .apprx.1.5.times.1010/cm2 eV for a 30 min SEG/epitaxial lateral overgrowth stress for nitrided oxides.
RE.CNT 35 THERE ARE 35 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 7 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:722923 HCAPLUS
DN 128:55872
TI An analytical symmetric **double-gate** silicon-on-insulator **metal-oxide-semiconductor field-effect-transistor** model
AU Jang, Sheng-Lyang; Hu, Man-Chun; Liu, Shau-Shen
CS National Taiwan University of Science and Technology, Taipei, 106, Taiwan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1997), 36(10), 6250-6253
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A new complete and anal. drain current model for sym. **double-gate Si**-on-insulator **metal-oxide-semiconductor field-effect-transistors** (**SOI MOSFETs**) is presented. The model applicable for digital/analog circuit simulation contains the following advanced features: precise description of the subthreshold, near threshold and above-threshold regions of operation by one single expression and consideration of the source/drain resistance. It includes important short channel effects such as velocity satn., drain induced barrier lowering and channel length modulation, self-heating effect due to the low thermal cond. of the buried oxide, and impact-ionization of **MOS** devices and parasitic bipolar junction transistor assocd. with drain breakdown. It was developed using a quasi-two-dimensional Poisson equation.

L32 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:252984 HCAPLUS
DN 132:259310
TI Method for making asymmetrical N-channel and symmetrical P-channel **semiconductor** devices
IN Gardner, Mark I.; Wristers, Derick J.; Fulford, H. Jim, Jr.
PA Advanced Micro Devices, Inc., USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6051471	A	20000418	US 1996-711957	19960903

AB An asym. N-channel IGFET and a sym. P-channel IGFET are disclosed. The N-channel IGFET includes heavily doped and ultra-heavily doped **source regions**, and lightly doped and heavily doped drain regions. The P-channel IGFET includes lightly doped and heavily doped **source** and drain **regions**. Forming the N-channel IGFET includes forming a **gate** with first and **second** opposing sidewalls, applying a first ion implantation to implant lightly doped N-type **source** and drain **regions**, applying a second ion implantation to convert the lightly doped N-type **source region** into a heavily doped N-type **source region** without doping the lightly doped N-type drain region, forming first and second spacers adjacent to the first and second sidewalls, resp., and applying a third ion implantation to convert a portion of the heavily doped N-type **source region** outside the first spacer into an ultra-heavily doped N-type **source region** without doping a portion of the heavily doped N-type **source region** beneath the first spacer, and to convert a portion of the lightly doped N-type drain region outside the second spacer into a heavily doped N-type drain region without doping a portion of the lightly doped N-type drain region beneath the second spacer. Advantageously, both IGFETs reduce hot carrier effects, and the N-channel IGFET has particularly low source-drain series resistance.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:75345 HCAPLUS
DN 126:219104
TI Fabrication of a new **Si** field emitter tip with **metal-oxide-semiconductor field-effect transistor** (**MOSFET**) structure
AU Hirano, Takayuki; Kanemaru, Seigo; Tanoue, Hisao; Itoh, Junji
CS Electrotechnical Laboratory, Tsukuba, 305, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1996), 35(12B), 6637-6640
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A current-controllable silicon field emitter tip with a **metal-oxide-semiconductor field-effect transistor** (**MOSFET**) structure is fabricated. The device has a simple structure in which a conical **Si** tip is made in the drain region of a **MOSFET**. The **gate** performs **two** roles; one is that of a conventional extn. gate and the other is that of a control gate for the drain current supplied to the tip. The fabrication process is very simple. In order to form n-type **regions** for the **source** and drain, only two steps including a self-aligned ion implantation were added to the conventional silicon tip fabrication process. Exptl. results showed that the emission current was well controlled and stabilized by the drain current of the **MOSFET**. Stable emission of about 0.8 .mu.A was obtained with a single tip. We also discuss a **dual-gate** **MOSFET** for further extension of the fabrication process introduced.

L35 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:487988 HCAPLUS
DN 137:55912
TI Surface breakdown reduction by internal field rings and multiple poly field plates in power LDMOSFET
IN Lin, Ming-Te
PA United Microelectronics Corp., USA
SO U.S. Pat. Appl. Publ., 4 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002079521	A1	20020627	US 2000-740805	20001221

AB The invention relates to a lateral double diffusion **metal oxide semiconductor field effect transistors** (LDMOSFET) utilizing internal field rings and poly field plates are proposed to enhance elec. characteristic of the power devices. At least one internal field ring is built in a **drift region** of the device to increase depletion capability of the **drift region**. The field plates are formed over and insulated from the **drift region** and preferably at least one of the field plates is designed to be positioned directly above each P/N junction created between the **drift region** and each internal field ring. These field plates according to the present invention are coupled to drain region of the LDMOSFET to facilitate elec. field distribution of the device. In our preferred embodiments, the field plates are made of polysilicon, the fabrication of which is similar to the formation of polysilicon gate layer in a typical **CMOS** process.

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File 315:ChemEng & Biotec Abs 1970-2002/Nov
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Set	Items	Description
S1	57	AU=(LETAVIC, T? OR LETAVIC T?)
S2	2148	AU=(SIMPSON, M? OR SIMPSON M?)
S3	14	S1 AND S2
S4	8	S3 AND SEMICONDUCT????????
S5	6	RD (unique items)
S6	6	S3 NOT S4
S7	5	S6 AND (HIGH()(VOLT? OR POWER?))
S8	4	RD (unique items)

8/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7412073 INSPEC Abstract Number: B2002-11-2570P-004
Title: A thin-layer **high-voltage** silicon-on-insulator hybrid LDMOS/LIGBT device
Author(s): Petruzzello, J.; **Letavic, T.**; van Zwol, H.; **Simpson, M.**; Mukherjee, S.
Author Affiliation: Philips Res. USA, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs (Cat. No.02CH37306) p.117-20
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xx+311 pp.
ISBN: 0 7803 7318 9 Material Identity Number: XX-2002-01938
U.S. Copyright Clearance Center Code: 0-7803-7318-9/02/$17.00
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs
Conference Sponsor: IEEE Electron Devices Soc.; Inst. Electr. Eng. Japan
Conference Date: 4-7 June 2002 Conference Location: Sante Fe, NM, USA
Language: English
Abstract: We present a new lateral **high-voltage** silicon-on-insulator (SOI) power device structure which is a hybrid combination of bipolar and unipolar current flow segments. The hybrid LDMOS/LIGBT device shows a substantial performance advantage over LDMOS due to voltage-dependent conductivity-modulation and a resultant increase in maximum source-follower current capability. When fabricated in an integrated SOI process flow, the LDMOS/LIGBT hybrid device reduces the power device area by 25-50% for many applications, resulting in cost-effective integration and miniaturization of power conversion systems that use a half-bridge topology.
Subfile: B

8/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7092180 INSPEC Abstract Number: B2001-12-2560R-133
Title: Lateral smart-discrete process and devices based on thin-layer silicon-on-insulator
Author(s): **Letavic, T.**; Petruzzello, J.; **Simpson, M.**; Curcio, J.; Mukherjee, S.; Davidson, J.; Peake, S.; Rogers, C.; Rutter, P.; Warwick, M.; Grover, R.
Author Affiliation: Philips Res. USA, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216) p. 407-10
Publisher: Inst. Electr. Eng. Japan, Tokyo, Japan
Publication Date: 2001 Country of Publication: Japan xxxi+467 pp.
ISBN: 4 88686 056 7 Material Identity Number: XX-2001-01446
Conference Title: Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01
Conference Sponsor: Inst. Electr. Eng. Japan
Conference Date: 4-7 June 2001 Conference Location: Osaka, Japan
Language: English
Abstract: A ten-mask lateral smart-discrete process technology which combines novel **high-voltage** RESURF transistor structures and a merged bipolar/DMOS process flow on thin-layer SOI substrates is presented. Benchmarking shows that 650 V/1.2 Ohm SOI lateral smart-discrete devices exhibit a total gate charge which is a factor-of-two lower than vertical super-junction devices, a temperature-independent body diode reverse recovery time which is a factor-of-two smaller than vertical ultra-fast silicon diodes, and total hard-switching losses which are lower than conventional VDMOS. The total gate charge, reverse recovery time, and switching delay times are the lowest reported values for 650 V silicon devices. This, in conjunction with a process with integrated logic, establishes SOI smart-discrete technology as best-in-class for efficient high-frequency power conversion.
Subfile: B

8/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6181690 INSPEC Abstract Number: B1999-04-1210-005
Title: 600 V single-chip power conversion system based on thin layer silicon-on-insulator
Author(s): **Letavic, T.**; Arnold, E.; **Simpson, M.**; Peters, E.; Aquino, R.; Egloff, R.; Wong, S.; Mukherjee, S.
Author Affiliation: Res. Lab., Philips Electron.North America Corp., Briarcliff Manor, NY, USA
Conference Title: 1998 IEEE International SOI Conference Proceedings (Cat No.98CH36199) p.133-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xi+174 pp.
ISBN: 0 7803 4500 2 Material Identity Number: XX-1998-02834
Conference Title: 1998 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 5-8 Oct. 1998 Conference Location: Stuart, FL, USA
Language: English
Abstract: Summary form only given. An integrated 600 V power conversion circuit is described based on smart power technology which combines novel lateral **high-voltage** RESURF transistor structures and a merged bipolar/CMOS/DMOS process flow on thin-layer SOI substrates. A modular process flow provides for the integration of half-bridge power stages along with level shifting and lowand medium-voltage control. This opens new application areas for thin-layer SOI, such as lighting electronics, power modules, motor control, etc., and is a significant development for the integration of power conversion systems.
Subfile: B

8/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5703883 INSPEC Abstract Number: B9711-2570K-001
Title: High performance 600 V smart power technology based on thin layer silicon-on-insulator
Author(s): **Letavic, T.**; Arnold, E.; **Simpson, M.**; Aquino, R.; Bhimnathwala, H.; Egloff, R.; Emmerik, A.; Wong, S.; Mukherjee, S.
Author Affiliation: Philips Electron. North American Corp., Briarcliff Manor, NY, USA
Conference Title: ISPSD '97. 1997 IEEE International Symposium on Power Semiconductor Devices and ICs (Cat. No.97CH36086) p.49-52
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 375 pp.
ISBN: 0 7803 3993 2 Material Identity Number: XX97-01367
U.S. Copyright Clearance Center Code: 0 7803 3993 2/97/$10.00
Conference Title: Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's
Conference Sponsor: VDE; IEEE Electron Devices Soc.; IEE Japan; EUREL
Conference Date: 26-29 May 1997 Conference Location: Weimar, Germany
Language: English
Abstract: A high-performance 600 V smart power technology has been developed in which novel lateral double-diffused MOS transistors (LDMOS) are merged with a BiCMOS process flow for the construction of power integrated circuits on bonded silicon-on-insulator (BSOI) substrates. All active and passive device structures have been optimized for fabrication on BSOI layers which are less than 1.5 mu m-thick, with buried oxide layers in the range of 2.0 to 3.0 mu m-thick. Complete dielectric isolation processing is straightforward due to the use of a thin SOI active device layer. A dual field plate design of the **high-voltage** devices results in at least a factor-of-two reduction in specific on-resistance over conventional LDMOS structures for a given breakdown voltage.
Subfile: B

5/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7412062 INSPEC Abstract Number: B2002-11-2560P-015
Title: Thin-layer silicon-on-insulator high-voltage PMOS device and application
Author(s): **Letavic, T.**; Albu, R.; Dufort, B.; Petruzzello, J.; **Simpson, M.**; Mukherjee, S.; Weijland, I.; van Zwol, H.
Author Affiliation: Philips Res. USA, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs (Cat. No.02CH37306) p.73-6
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xx+311 pp.
ISBN: 0 7803 7318 9 Material Identity Number: XX-2002-01938
U.S. Copyright Clearance Center Code: 0-7803-7318-9/02/$17.00
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs
Conference Sponsor: IEEE Electron Devices Soc.; Inst. Electr. Eng. Japan
Conference Date: 4-7 June 2002 Conference Location: Sante Fe, NM, USA
Language: English
Abstract: We present a thin-layer silicon-on-insulator (SOI) high-voltage PMOS device structure and measured performance characteristics. The all-implanted device structure supports voltage by multi-dimensional depletion from a combination of implanted surface pn junctions and MOS capacitor structures formed with multi-level dielectric deposition and metallization. A graded-doped body region has been optimized for application voltages from 100-600 V, and the structure has been evaluated in applications including high-voltage level shifting, low-dissipation bias networks, and high-voltage high-frequency class AB power output stages. The integrated high-voltage PMOS device structure enables low-power, high voltage, and high-speed complementary circuit topologies to be realized in a thin-layer SOI process flow, improving circuit efficiency and expanding the application base for thin-layer technology.
Subfile: B

5/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6475749 INSPEC Abstract Number: B2000-02-1210-052
Title: 600 V power conversion system-on-a-chip based on thin layer silicon-on-insulator
Author(s): **Letavic, T.**; **Simpson, M.**; Arnold, E.; Peters, E.; Aquino, R.; Curcio, J.; Herko, S.; Mukherjee, S.
Author Affiliation: Philips Res., Philips Electron. North America Corp., Briarcliff Manor, NY, USA
Conference Title: 11th International Symposium on Power Semiconductor Devices and ICs. ISPSD'99 Proceedings (Cat. No.99CH36312) p.325-8
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xxiii+359 pp.
ISBN: 0 7803 5290 4 Material Identity Number: XX-1999-02322
U.S. Copyright Clearance Center Code: 0 7803 5290 4/99/$10.00
Conference Title: 11th International Symposium on Power Semiconductor Devices and ICs. ISPSD '99
Conference Sponsor: IEEE Electron Devices Soc.; Inst. Elec. Eng. of Japan
Conference Date: 26-28 May 1999 Conference Location: Toronto, Ont., Canada
Language: English
Abstract: An integrated 600 V power conversion system is described based on smart power technology which combines novel lateral high-voltage RESURF transistor structures and a merged bipolar/CMOS/DMOS process flow on thin-layer SOI substrates. A new high-voltage SOI LDMOS device structure is presented which results in a factor-of-two decrease in specific on-resistance and a factor-of-two improvement in source-follower saturated current, thus overcoming a key limitation of integrated thin-layer technology. This opens new application areas for thin-layer SOI, such as lighting electronics, power modules, motor control, and others, a significant development for the integration of power conversion systems.
Subfile: B

5/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05930449
E.I. No: EIP01446710200
Title: Lateral smart-discrete process and devices based on thin-layer silicon-on-insulator
Author: **Letavic, T.**; Petruzzello, J.; **Simpson, M.**; Curcio, J. ; Mukherjee, S.; Davidson, J.; Peake, S.; Rogers, C.; Rutter, P.; Warwick, M.; Grover, R.
Corporate Source: Philips Research USA, Briarcliff Manor, NY 10510, United States
Conference Title: 13th International Symposium on Power Semiconductor Devices and ICs (ISPSD'01)
Conference Location: Osaka, Japan Conference Date: 20010604-20010607
E.I. Conference No.: 58615
Source: IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2001. p 407-410 (IEEE cat n 01CH37216)
Publication Year: 2001
CODEN: PISDEK
Language: English
Abstract: A ten-mask lateral smart-discrete process technology which combines novel high-voltage RESURF transistor structures and a merged bipolar/DMOS process flow on thin-layer SOI substrates is presented. Benchmarking shows that 650V/1.2 Ohm SOI lateral smart-discrete devices exhibit a total gate charge which is a factor-of-two lower than vertical super junction devices, a temperature-independent body diode reverse recovery time which is a factor-of-two smaller than vertical ultra-fast silicon diodes, and total hard-switching losses which are lower than conventional VDMOS. The total gate charge, reverse recovery time, and switching delay times are the lowest reported values for 650V silicon devices. This, in conjunction with a process with integrated logic, establishes SOI smart-discrete technology as best-in-class for efficient high-frequency power conversion. 8 Refs.

5/3,AB/4 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05413027
E.I. No: EIP99114893857
Title: 600V power conversion system-on-a-chip based on thin layer silicon-on-insulator
Author: **Letavic, T.**; **Simpson, M.**; Arnold, E.; Peters, E.; Aquino, R.; Curcio, J.; Herko, S.; Mukherjee, S.
Corporate Source: Philips Electronics North America Corp, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 1999 11th International Symposium on Power Semiconductor Devices and IC's, ISPSD'99
Conference Location: Toronto, Ont, Can Conference Date: 19990526-19990528
E.I. Conference No.: 55507
Source: IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) 1999. p 325-328
Publication Year: 1999
CODEN: PISDEK
Language: English
Abstract: An integrated 600 V power conversion system is described based on smart power technology which combines novel lateral high-voltage RESURF transistor structures and a merged Bipolar/CMOS/DMOS process flow on thin-layer SOI substrates. A new high-voltage SOI LDMOS device structure is presented which results in a factor-of-two decrease in specific on-resistance and a factor-of-two improvement in source-follower saturated current, thus overcoming a key limitation of integrated thin-layer technology. This opens new application areas for thin-layer SOI, such as lighting electronics, power modules, motor control, and others, a significant development for the integration of power conversion systems. (Author abstract) 5 Refs.

5/3,AB/5 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04814964
E.I. No: EIP97093816238
Title: High performance 600 V smart power technology based on thin layer silicon-on-insulator
Author: **Letavic, T.**; Arnold, E.; **Simpson, M.**; Aquino, R.; Bhimnathwala, H.; Egloff, R.; Emmerik, A.; Wong, S.; Mukherjee, S.
Corporate Source: Philips Electronics North America Corp, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 1997 9th International Symposium on Power Semiconductor Devices and ICs, ISPSD
Conference Location: Weimer, Ger Conference Date: 19970526-19970529
E.I. Conference No.: 46957
Source: IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD) 1997. IEEE, Piscataway, NJ, USA,97CH36086. p 49-52
Publication Year: 1997
CODEN: PISDEK
Language: English
Abstract: A high-performance 600 V smart power technology has been developed in which novel lateral double-diffused MOS transistors (LDMOS) are merged with a BiCMOS process flow for the construction of power integrated circuits on bonded silicon-on-insulator (BSOI) substrates. All active and passive device structures have been optimized for fabrication on BSOI layers which are less than 1.5 mu m-thick, with buried oxide layers in the range of 2.0 to 3.0 mu m-thick. Complete dielectric isolation processing is straightforward due to the use of a thin SOI active device layer. A dual field plate design of the high-voltage devices results in at least a factor-of-two reduction in specific on-resistance over conventional LDMOS structures for a given breakdown voltage. (Author abstract) 10 Refs.

5/3,AB/6 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

04210125 INSIDE CONFERENCE ITEM ID: CN044168868
A thin-layer high-voltage silicon-on-insulator hybrid LDMOS/LIGBT device
Petruzzello, J.; **Letavic, T.**; van Zwol, H.; **Simpson, M.**;
Mukherjee, S.
CONFERENCE: International symposium on power semiconductor devices & ICs -14th
PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON POWER SEMICONDUCTOR DEVICES AND ICS-IEEE, 2002; 14TH P: 117-120
IEEE, 2002
ISBN: 0780373189
LANGUAGE: English DOCUMENT TYPE: Conference Papers and programme
CONFERENCE LOCATION: Santa Fe, NM 2002; Jun (200206) (200206)
NOTE:
IEEE cat no: 02CH37306